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Continuing Education Course #625
Electronics
Course III Miscellany Devices

1. What is the condition of a transistor given the following information?

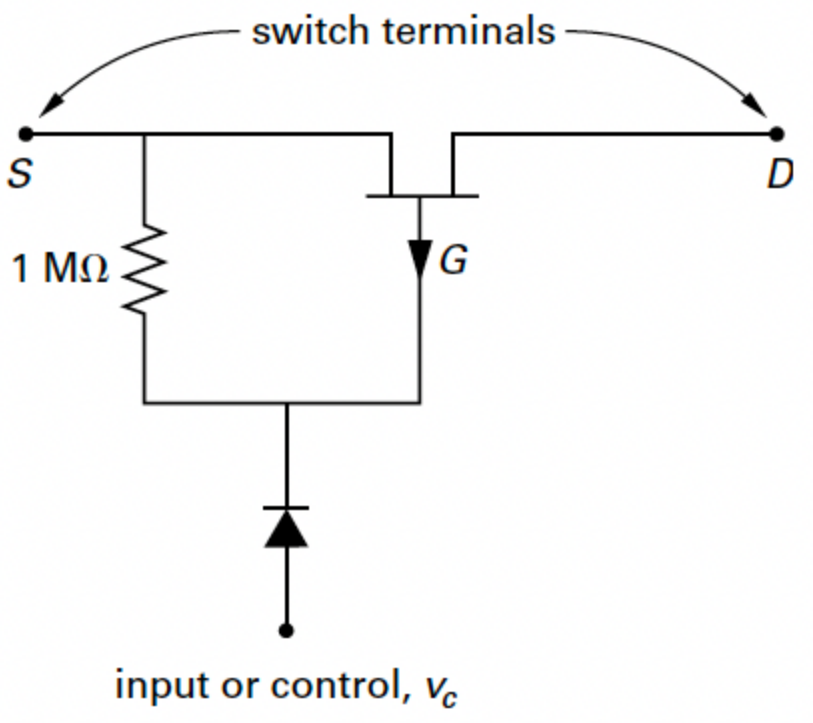
Collector Supply Voltage: 12 V
Load Resistance: 400 Ω
I_{base} = 0 A

- a. active
- b. off
- c. on
- d. saturated

2. When a transistor is ON, the base-emitter junction is ____ biased and the collector base junction is _____ biased.

- a. forward / forward
- b. forward / reversed
- c. reversed / forward
- d. reversed / reversed

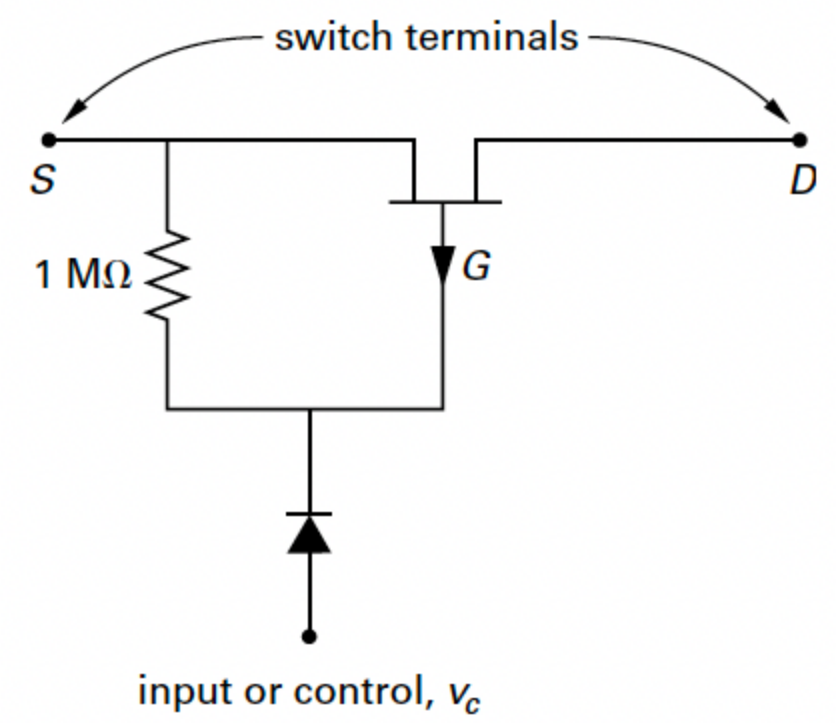
3. Consider the circuit shown.



If the control voltage, v_C, is zero, what is the status of the JFET switch?

- a. off
- b. on
- c. neither
- d. depends on the resistance

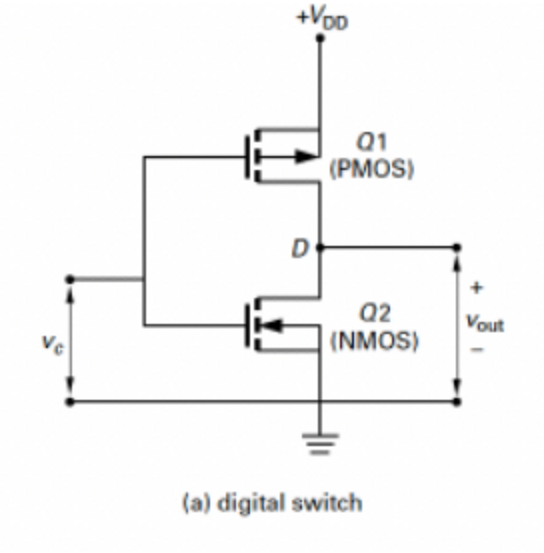
4. Consider the circuit shown.



The direction of the arrow on the gate indicates a _____ to _____ junction.

- a. n to p
- b. p to n
- c. n to n
- d. p to p

5. Consider the circuit shown.



(a) digital switch

When the control voltage, vc, is 0 V, Q1 is _____ and Q2 is _____.

- a. off / off
- b. off / on
- c. on / on
- d. on / off

6. What is a primary advantage of CMOS circuitry?

- a. low costs
- b. low current flow
- c. low packing density
- d. low power requirements

7. Consider the gate shown.

What input to the gates A and B result in a zero output?

- a. 00
- b. 01
- c. 10
- d. 11

8. Consider that logic gate shown.

For inputs A and B, what formula symbolizes the output?

- a. AB
- b. A+B
- c. $\overline{AB}$
- d. $A \oplus B$

9. What rule of Boolean algebra is shown?

$A + (A \cdot B) = A$
$A \cdot (A + B) = A$

- a. absorptive
- b. associative
- c. commutative
- d. distributive

10. What is the equivalent result of the following?

$\overline{A + B}$

- a. $\overline{A} \cdot \overline{B}$
- b. $A \cdot B$
- c. $A + B$
- d. $\overline{A \cdot B}$

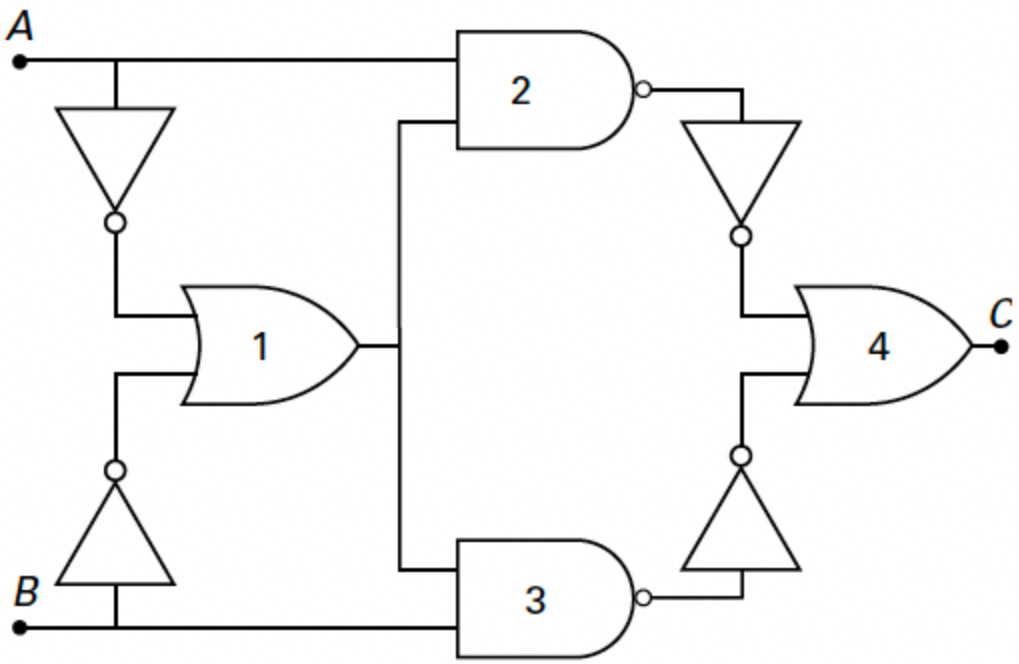
11. Consider the following identities.

$A + 0 =$
$A + 1 =$
$A + A =$
$A + \overline{A} =$

In order, from top to bottom, what are the values of the identities?

- a. A, 1, A, 1
- b. 0, 1, A, 0
- c. 0, 1, 0, 1
- d. 1, A, 1, A

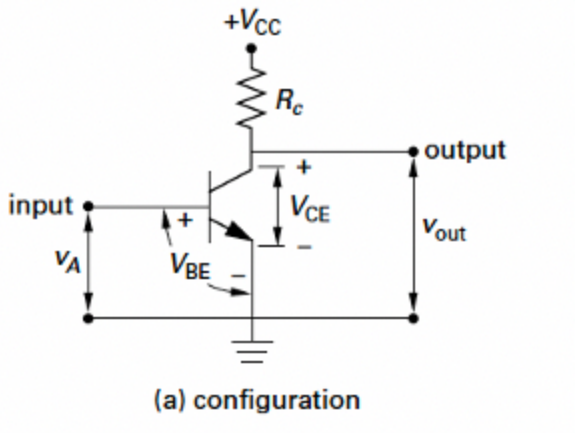
12. Consider the gates shown.



What is the output of gate 2?

- a. $\overline{A \cdot (A + \overline{B})}$
- b. $\overline{A \cdot (\overline{A} + B)}$
- c. $\overline{A \cdot (\overline{A} + \overline{B})}$
- d. $\overline{A \cdot (\overline{A} + \overline{B})}$

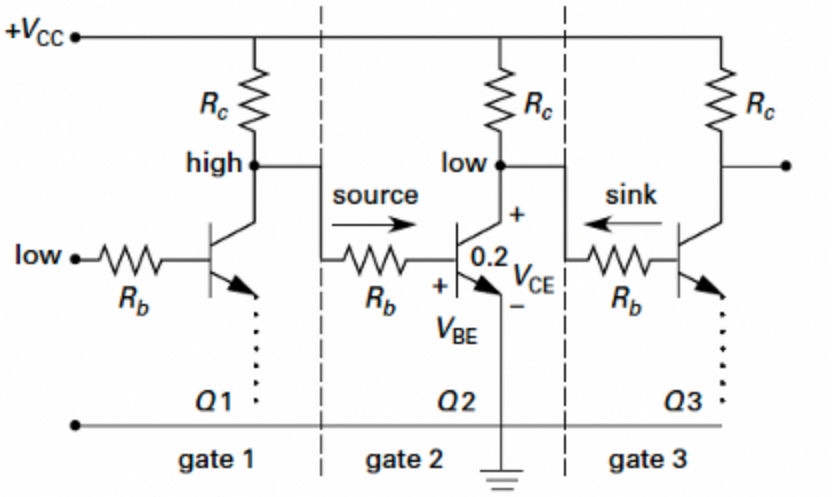
13. Consider the circuit shown.



What type of gate is represented?

- a. NOT
- b. NAND
- c. NOR
- d. none of the above

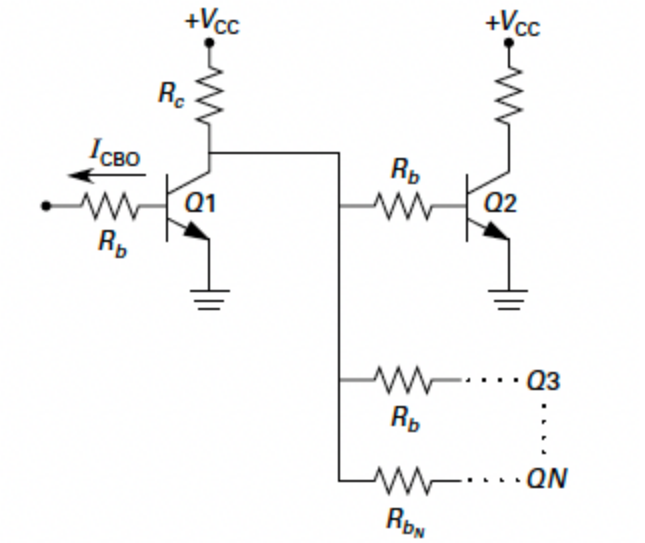
14. Consider the circuit shown.



What is the formula for the unit source current for Q2?

- a. $I_{B2} = \dfrac{V_{CC} - V_{BE2}}{R_c}$
- b. $I_{B2} = \dfrac{V_{CC} - V_{BE2}}{R_c + R_b}$
- c. $I_{B2} = \dfrac{V_{CC} - V_{CE2}}{R_c + R_b}$
- d. $I_{B2} = \dfrac{V_{CC} - V_{BE2}}{R_b}$

15. Consider the circuit shown.



Parameters taken from a manufacturer's data sheet indicate that V_{CC} = 5.0 V, $I_{B,sat}$ > 0.5 mA, $V_{BE,sat}$ <1.5 V, R_c = 500 Ω, and R_b = 1000 Ω.

By how much does a reverse saturation current of 1 mA lower the fan-out of Q1?

HINT: Model Q2 as OPEN, KCL from $+V_{CC}$ to emitter Q2 ground. Solve for N. Then Eq. 45.

- a. 2
- b. 4

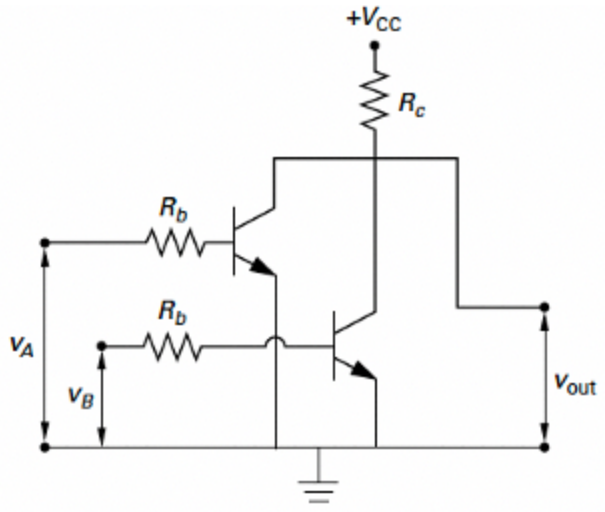
○ c. 10
○ d. 12

16. A particular logic gate has the following parameters: t_d = 5 ns, t_r = 50 ns, t_s = 30 ns, and t_f = 30 ns.

What is the maximum frequency at which this gate can operate?
○ a. 8.7 µHz
○ b. 8.7 MHz
○ c. 60 MHz
○ d. 115 MHz

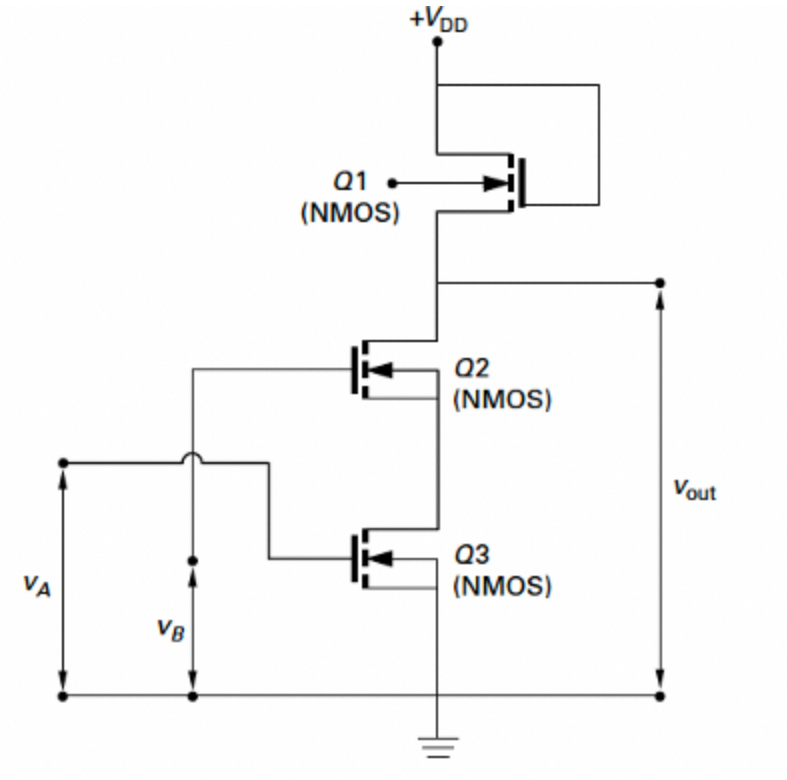
17. Which logic family has the greatest fan-out and least propagation delay?
○ a. CMOS
○ b. ECL
○ c. MOS
○ d. TTL

18. What type of RTL gate is shown?



○ a. AND
○ b. NOR
○ c. NAND
○ d. OR

19. What type of MOS logic is shown?

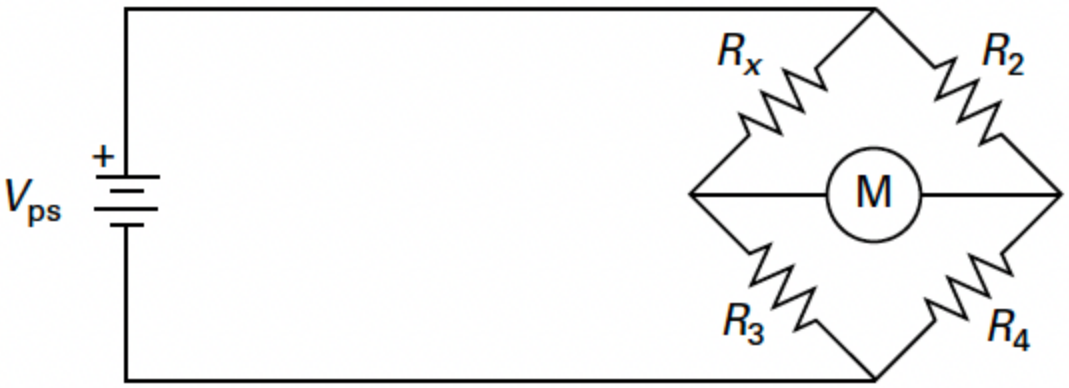


- a. AND
- b. NOR
- c. NAND
- d. OR

20. What type of multivibrator may be used as a digital system clock?
- a. astable
- b. bistable
- c. monostable
- d. none of the above

21. What type of RTD bridge is the most accurate?
- a. one-wire
- b. two-wire
- c. three-wire
- d. four-wire

22. A portion of a ground detection circuit is shown.



Resistor R2 has a value of 1 kΩ. Resistors R3 and R4 have values of 10 kΩ and 2 kΩ, respectively. The power-supply voltage of the circuit is 24 V. The meter is designed to deflect fully to the right on the scale face, indicating â€œsatisfactoryâ€ (i.e., no ground) when 0 A passes through the meter.

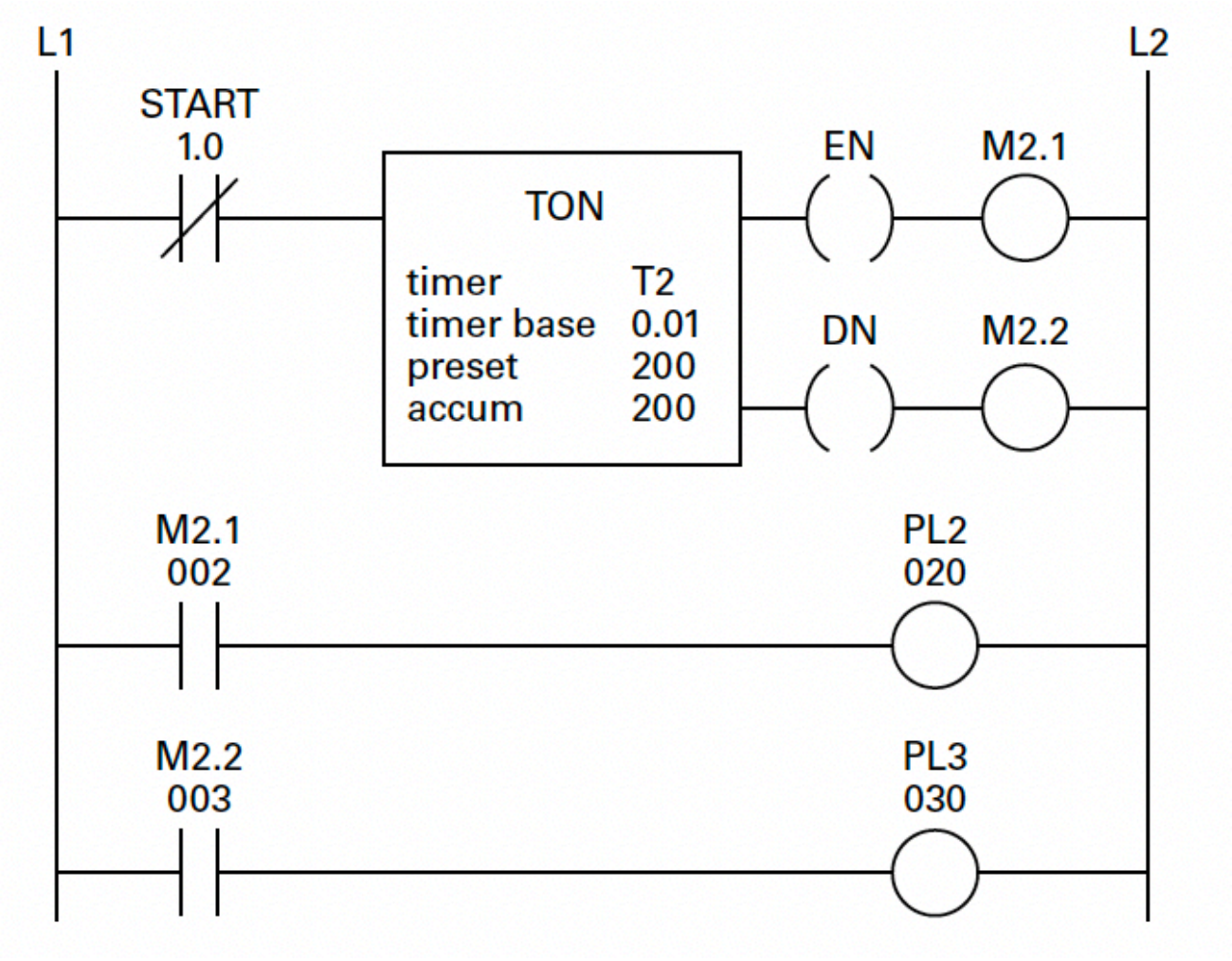
What is most nearly the resistance value, Rx, necessary to result in a no-ground condition?

- a. 200 Ω
- b. 1000 Ω
- c. 5000 Ω
- d. 10,000 Ω

23. Programmable Logic Controllers use _____ logic that represent _____ the designing engineer wants followed.

- a. CMOS / Formulas
- b. ECL / Rules
- c. Ladder / Rules
- d. TTL / Formulas

24. A portion of the program coding for a PLC application is shown. The input line is hot.

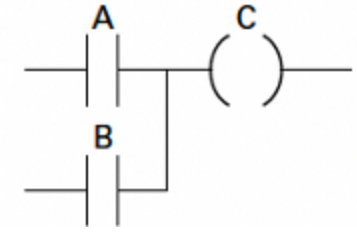


Given the status of the timer, which relays are energized?

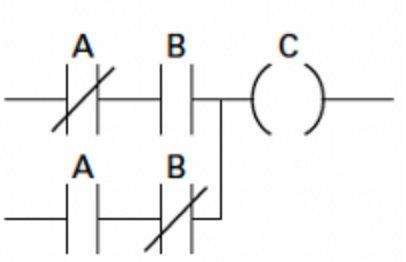
- a. M2.1 / PL2
- b. M2.1 / PL3
- c. M2.2 / PL3
- d. M2.1 / M2.2 / PL2 / PL3

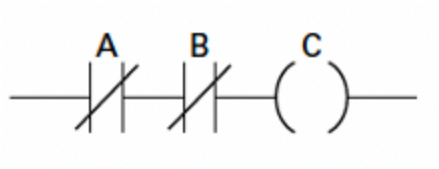
25. What ladder logic represents a NAND gate?

a.



b.



○ c. 

○ d.