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Continuing Education Course #519
Digital Design: Combinational Logic

1. The twos' complement of the decimal number 84 (0x54 in hexadecimal) is
- a. 10100011
- b. 10110101
- c. 10101100
- d. 11001011

2. Using Boolean algebra, simplify the expression (A' + B)'.
- a. AB'
- b. A + B'
- c. A'B
- d. A' + B

3. Convert the binary number 1110001011000111
- a. 0xBC35
- b. 0x8613
- c. 0xD2C3
- d. 0xE2C7

4. Using Boolean algebra, simplify the expression AB + ABC.
- a. C
- b. AB
- c. ABC
- d. BC

5. Using Boolean algebra, simplify the expression (A' + B')(A + B').
- a. B'
- b. A'
- c. A'B' + AB'
- d. A + B

6. The binary approximation of the decimal number 137.57 is
- a. 10001001.010111001
- b. 10101100.101010010
- c. 10101100.011011011
- d. 10001001.100100011

7. The fundamental logic gates are _____________.
- a. NAND, NOR
- b. AND, OR, NOT

○ c. XOR, NAND, NOR
○ d. OR, NOR, XOR, XNOR

8. An XOR function yields the expression ____________.
○ a. AB
○ b. A + B
○ c. A’B + AB’
○ d. (AB)’

9. Convert the product-of-sums (A + B)(A’ + C) to a sum-of-products by distributing the terms.
○ a. AC + BC
○ b. AC + A’B + BC
○ c. AA’ + A’B + BC
○ d. BB’ + C

Figure A1

A	B	C	F
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	0

10. The truth table in Figure A1 describes the expression ____________.
○ a. A’B’C’ + A’BC’ + ABC
○ b. A’BC + AB’C
○ c. A’BC’ + ABC’
○ d. A’B’C + A’BC’ + ABC’

11. In order to simplify an expression that contains 4 variables, a Karnaugh map can be used that has a ____________ grid.
○ a. 2 x 2
○ b. 2 x 4
○ c. 4 x 8
○ d. 4 x 4

Figure A2

A \ BC	00	01	11	10
0	1	1	0	0
1	1	1	1	0

12. The Karnaugh map in Figure A2 is associated with the (non-optimal) expression ____________.

- ◯ a. F = A’B’C’ + A’BC’ + AB’C + ABC’
- ◯ b. F = A’B’C’ + A’B’C + AB’C’ + AB’C + ABC
- ◯ c. F = A’B’C + AB’C’ + AB’C
- ◯ d. F = A’BC’ + A’BC + ABC’

13. The Karnaugh map in Figure A2 yields the optimal expression ____________.
- ◯ a. F = A’ + BC
- ◯ b. F = A’B + BC’
- ◯ c. F = B’ + AC
- ◯ d. F = AC’

Figure A3

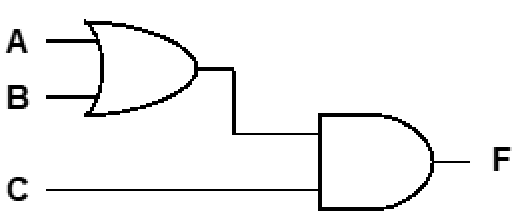
A \ BC	00	01	11	10
0	0	1	1	1
1	0	1	1	1

14. The Karnaugh map in Figure A3 yields the optimal expression ____________.
- ◯ a. F = B’C + BC + BC’
- ◯ b. F = B + C
- ◯ c. F = A + B + C
- ◯ d. F = AB + BC

15. Convert the hexadecimal number 0xAB83 to binary
- ◯ a. 1011100100010011
- ◯ b. 1010101110000011
- ◯ c. 1110001110101001
- ◯ d. 1011000101101010

16. ____________ gates have functional completeness. This means that any logic function can be realized using only this gate.
- ◯ a. AND
- ◯ b. OR
- ◯ c. NAND
- ◯ d. XOR

Figure A4

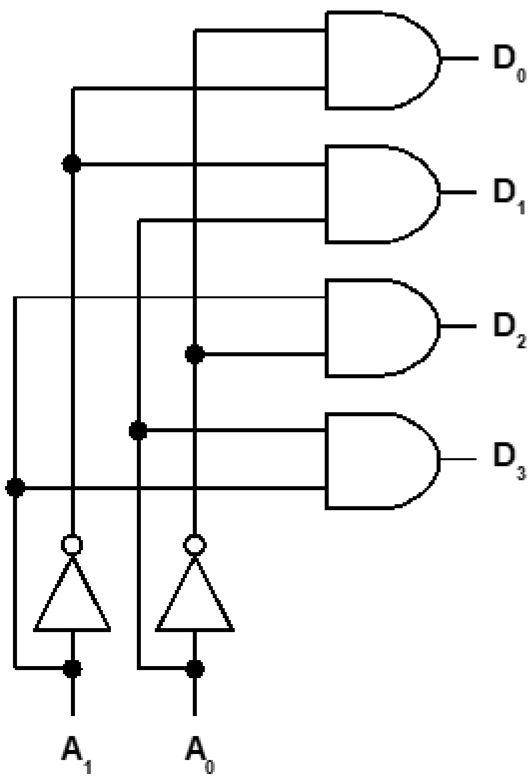


17. The combinational logic diagram in Figure A4 produces the expression ____________.
- ◯ a. AB + C
- ◯ b. A + B + C

○ c. ABC
○ d. F = (A + B)C

18. A demultiplexer is different from a decoder because ____________.
○ a. only a decoder has select lines
○ b. a demultiplexer has a data input while a decoder does not
○ c. a demultiplexer does not have any output
○ d. there is no difference

Figure A5



19. For a 2-to-4 decoder in Figure A5, an output of D3D2D1D0 of 0100 would result with an input of A1A0 of ____________.
○ a. 11
○ b. 00
○ c. 10
○ d. 01

20. For the 2-to-4 decoder in Figure A5, an output of ____________ would result with an input of A1A0 equal to 00.
○ a. D0 = 1
○ b. D1 = 1
○ c. D2 = 1
○ d. D3 = 1

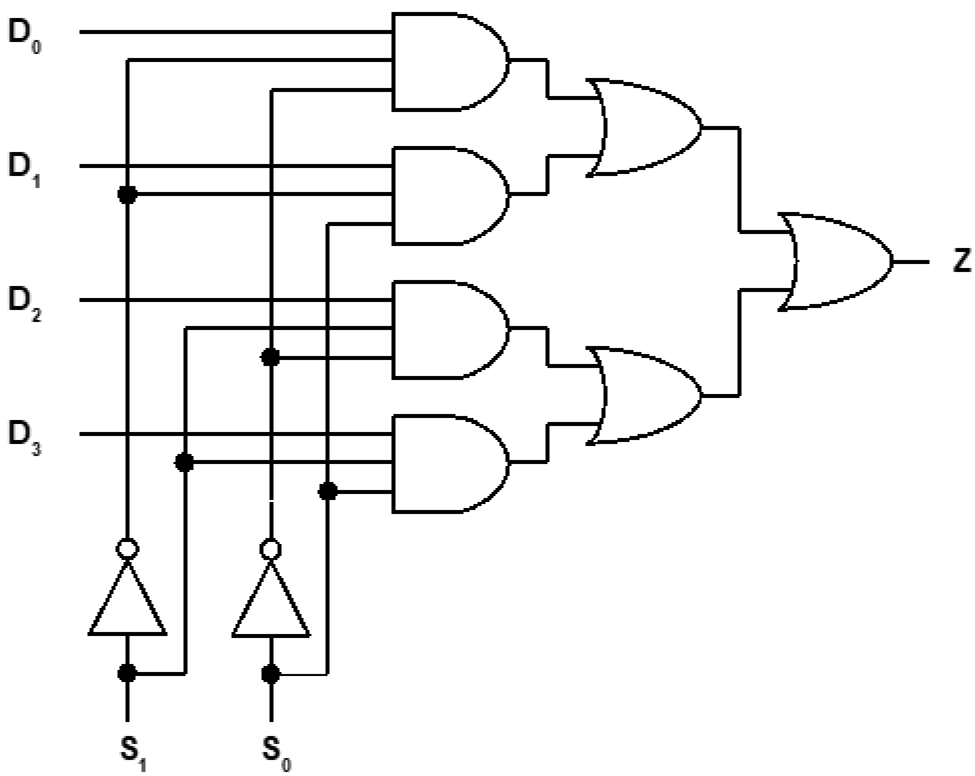
21. A 4-to-1 multiplexer has ____________ inputs using 2 data select lines.
○ a. 4
○ b. 1

○ c. 2
○ d. 8

22. A ____________ is used in digital systems to select a particular data path to be processed or stored. They allow several signals to share one resource like a data bus.
○ a. demultiplexer
○ b. decoder
○ c. adder
○ d. multiplexer

23. A ____________ takes a single input and routes it to one of many outputs. It is the opposite of a multiplexer.
○ a. decoder
○ b. encoder
○ c. demultiplexer
○ d. full adder

Figure A6



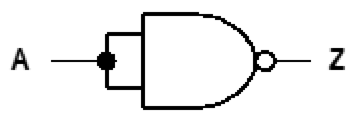
24. For the 4-to-1 multiplexer in Figure A6, what input on the data select lines S1S0 will route the input D2 to the output Z?
○ a. 01
○ b. 11
○ c. 10
○ d. 00

25. For the 4-to-1 multiplexer in Figure A6, an input of 11 will route which input to the output Z.
○ a. D2
○ b. D3

- c. D0
- d. D1

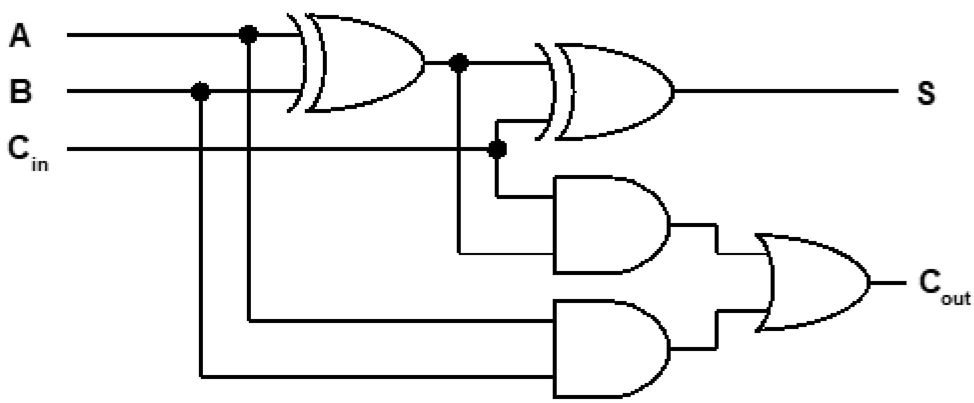
26. An adder that has two inputs A and B has two outputs, S (sum) and ____________?
- a. subtract
- b. add
- c. remainder
- d. carry

Figure A7



27. The logic diagram in Figure A7 implements which basic logic function?
- a. AND
- b. NOT
- c. OR
- d. XOR

Figure A8



28. The logic diagram in Figure A8 is for a full adder. For an input of A = 1, B = 1, Cin = 0, the output will be ____________.
- a. Cout = 0, S = 1
- b. Cout = 0, S = 0
- c. Cout = 1, S = 0
- d. Cout = 1, S = 1

29. For the full adder in Figure A8, an input of A = 0, B = 0, Cin = 1 will produce an output of ____________.
- a. Cout = 1, S = 0
- b. Cout = 0, S = 0
- c. Cout = 1, S = 1
- d. Cout = 0, S = 1

30. Adders can be connected together in a cascaded format starting with a half adder for the least significant bit then followed by multiple full adders ending with the most significant bit. This will allow binary numbers larger than one bit to be added together. This device is called a ____________.

- ○ a. ripple carry adder
- ○ b. half adder
- ○ c. full adder
- ○ d. decoder