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Continuing Education Course #112
Memories in Computers
Part 3: Flash Memories

1. Who is credited with the invention of nonvolatile memory?
- a. Kahng & Sze
- b. Masuoka
- c. Momodomi
- d. Fulford
- e. Prince

2. What company commercialized flash memory?
- a. Toshiba
- b. Intel
- c. AMD
- d. Bell Labs

3. Why is flash memory important?
- a. Lower cost per bit than DRAM
- b. Higher density per chip than DRAM
- c. Nonvolatile, unlike DRAM which is volatile
- d. None of the above
- e. All of the above

4. What is the approximate data retention time for a flash memory?
- a. 100 milliseconds
- b. 1 week
- c. 1 year
- d. 10 years
- e. Flash retains data forever

5. How are electrons moved through the insulator to the floating gate in a flash memory cell?
- a. Electrons are implanted there during manufacture
- b. Hot electron injection
- c. Cryogenic conduction
- d. It is not possible to move electrons through an insulator

6. What is one of the problems with Fowler-Nordheim tunneling?
- a. High source-drain current usually requires an off-chip high voltage power supply.
- b. Over-erasure so transistor becomes depletion mode
- c. Cannot be used for erasing
- d. Requires a dedicated erase electrode

7. What is the purpose of the series transistor in a split gate memory cell structure?

○ a. It provides control of the hot electron injection process.
○ b. It provides electrons for the Fowler-Nordheim tunneling process.
○ c. It connects the bit line to the device drain.
○ d. It prevents conduction of the floating gate transistor in case it is over-erased.

8. What is the advantage of using Fowler-Nordheim tunneling for both programming and erasing?

○ a. It reduces stress on the thin gate oxide.
○ b. Sending electrons both ways eliminates trap states.
○ c. The low current requirement allows on-chip high voltage generation.
○ d. Erasing using F-N tunneling is easier to control.

9. What does the term endurance mean when applied to flash memories?

○ a. Endurance is the amount of time data can be stored in a flash memory.
○ b. Endurance is the number of program/erase cycles a flash memory is capable of.
○ c. Endurance is the number of read cycles a flash memory is capable of.
○ d. Endurance is the power supply voltage range a flash memory can survive.

10. What steps have been taken to compensate for the wearout mechanisms inherent in flash memories?

○ a. Because the number of erase and program operations that any given cell has experienced is unpredictable, the success of the next such operation is also unpredictable. So it is standard practice to read data from the flash memory cell immediately after erasing or programming it to verify that the operation has been successful. The data from that cell reading is compared internally to the desired data, and is not conveyed to the memory output terminals as it would be in an actual memory read operation.
○ b. Program and erase algorithms that minimize oxide stress have been developed. For example, erasing and programming might be done in smaller incremental steps with verification after each step. Once the verification is satisfied, erasing or programming is stopped; thus reducing oxide stress.
○ c. Spare regions of memory are provided to replace areas that have received excessive program-erase cycles, as evidenced by failed verification.
○ d. Devices and systems utilize error detection and correction schemes.
○ e. None of the above.
○ f. All of the above.

11. In a NOR array, how are the memory cells arranged?

○ a. Every cell is individually addressable, as in a DRAM.
○ b. Multiple cells are in series between select gate transistors.
○ c. Cells are placed only where “1’s” are to be stored.
○ d. Cells are placed as close together as possible.

12. What happens if the erase verify operation finds that not all cells were erased properly?

○ a. Additional voltage pulses of the same amplitude are applied.
○ b. Additional voltage pulses of a different amplitude are applied.
○ c. Additional voltage pulses of the same duration are applied.
○ d. Additional voltage pulses of a different duration are applied.
○ e. Nothing further is done, as erasing failed.
○ f. Nothing further is done, as some cells can never be erased.
○ g. Any of answers (a) through (d) can be done, depending on the specific device.

13. In a NOR array, which cells have to be programmed?

○ a. Only those cells that are to store a “1.”
○ b. Every cell must be programmed to the desired level.

○ c. Only those cells intended to store a “0.”

14. When reading a flash memory, what happens to the data stored in the cells?
○ a. Readout is destructive, as in a DRAM, and must be restored.
○ b. It depends on what the data is; “0’s” are destroyed and “1’s” are retained.
○ c. It depends on what the data is; “1’s” are destroyed and “0’s” are retained.
○ d. Readout is non-destructive, so no restoration is required.

15. In a NAND array, how are the memory cells arranged?
○ a. Every cell is individually addressable, as in a DRAM.
○ b. Multiple cells are in series between select gate transistors.
○ c. Cells are placed only where “1’s” are to be stored.
○ d. Cells are placed as close together as possible.

16. How does the area of a NAND array compare to that of a NOR array, assuming the same number of memory cells and the same design rules?
○ a. The NAND array requires 40% more area than a NOR array.
○ b. They are the same size.
○ c. The NAND array requires 40% of the area of a NOR array.
○ d. Need more data to answer this question.

17. In a NAND array, what is the threshold voltage of erased cells?
○ a. Negative, so they will conduct with zero gate voltage
○ b. Anything below V_{DD}, as the series transistor prevents conduction.
○ c. Above V_{DD}/, so they can later be programmed.
○ d. Exactly zero.
○ e. About V_{DD}/2.

18. In a NAND array, what is the threshold voltage of programmed cells?
○ a. Negative, so they will conduct with zero gate voltage
○ b. Anything below V_{DD}, as the series transistor prevents conduction.
○ c. Above V_{DD}/, so they can later be erased.
○ d. Exactly zero.
○ e. About V_{DD}/2.

19. What voltages are applied to the word lines when reading from a NAND array?
○ a. All word lines except the selected one are kept at 0V, and the selected word line is driven to V_{DD}, just like a DRAM.
○ b. All word lines except the selected one are driven to V_{DD}, and the selected word line is at 0V.
○ c. All word lines except the selected one are driven to V_{DD} /2, and the selected word line is driven to V_{DD}.
○ d. All word lines except the selected one are driven to V_{DD} /2, and the selected word line is at 0V.

20. Comparing NOR and NAND arrays, for which of the following applications is NOR better?
○ a. Random code execution.
○ b. Personal music player (e.g., iPod).
○ c. Sequential data storage.
○ d. Anything requiring fast block erase.

21. What is the smallest erasable unit in a NOR array flash memory?

- a. Bit
- b. Byte
- c. Page
- d. Block
- e. Array

22. Why do most commands for the NOR flash device discussed in Section F require two cycles?
- a. To specify the row and then the column address.
- b. The first command identifies the device being addressed; the second tells it what to do.
- c. To prevent accidental erasure or programming.
- d. The first command selects the block; the second command selects the byte.

23. For the NOR flash device discussed in Section F, what is the level of VPEN for an Array Write operation?
- a. It must be low.
- b. It is “Don’t Care” for Array Write.
- c. It must be high.

24. Relative to the address inputs, how does a NAND array flash device differ from a NOR array flash device?
- a. They are the same.
- b. NOR devices do not have dedicated address pins; NAND devices do.
- c. NAND devices do not have dedicated address pins; NOR devices do.

25. What is the smallest erasable unit in a NAND array flash memory?
- a. Bit
- b. Byte
- c. Page
- d. Block
- e. Array

26. What is the smallest programmable unit in a NAND array flash memory?
- a. Bit
- b. Byte
- c. Page
- d. Block
- e. Array

27. In the NAND array device discussed in Section G, at what time are commands written to the device?
- a. Whenever an address changes (ATD circuit).
- b. When CLK rises.
- c. When CLK falls.
- d. When CE# falls.
- e. When WE# rises.

28. DC voltage boosting by use of a charge pump involves what circuit element?
- a. Inductor
- b. Transformer
- c. Capacitor
- d. Memristor

29. What is the common factor in all charge pump circuits?

○ a. All contain transformers.
○ b. All result in a voltage of opposite polarity relative to the power supply.
○ c. All require a conversion of DC to AC.
○ d. All are built on integrated circuits.

30. What is the essential factor permitting design of multi-level storage flash memory cells?
○ a. Fowler-Nordheim tunneling is an inherently precise mechanism.
○ b. Redundancy permits replacing bad rows or columns of memory.
○ c. Moore's Law permits the resulting doubling of chip storage density.
○ d. Charge on the floating gate does not leak off.

31. How many different threshold voltages are required to achieve multi-level storage?
○ a. One
○ b. Two
○ c. Three
○ d. Four
○ e. Six
○ f. Eight

32. What are two characteristics of multi-level storage as compared to single level storage?
○ a. Multi-level storage has much poorer endurance and much higher error rate.
○ b. Multi-level storage has longer programming times and shorter page transfer times.
○ c. Multi-level storage has longer page transfer times and better endurance.
○ d. Multi-level storage requires 12 correctable bits per 512 bytes and has shorter programming times.

33. A Hamming Code can correct all double-bit errors.
○ a. True
○ b. False

34. Name three error correcting codes.
○ a. Fowler-Nordheim, Hamming and FCA
○ b. Hamming, Reed-Solomon and BCH
○ c. MPU, HEI and ECC
○ d. MLC, SLC and Fowler-Nordheim

35. About how many bytes of NAND flash memory were sold in 2010?
○ a. 10^{16}
○ b. 10^{17}
○ c. 10^{18}
○ d. 10^{19}

36. What was Intel's flash memory market share in 1995?
○ a. 75%
○ b. 42%
○ c. 26%
○ d. 11%

37. In what year was the first removable flash memory card introduced?
○ a. 1976
○ b. 1994

○ c. 2002
○ d. 2006

38. What popular computer comes equipped with a 64 GB solid state drive?
○ a. Toshiba Mini
○ b. Apple MacBook Air
○ c. HP Pavilion
○ d. Sony Vaio

39. What is the binary equivalent of 33h?
○ a. 51
○ b. 0001 0011
○ c. 0011 0011
○ d. 0011 0010