Visit Suncam.com for more courses

Continuing Education Course #111
Memories in Computers
Part 2: DDR SDRAMs

1. What initiates an operation in an SDRAM?
- a. RAS# transitioning high to low
- b. CAS# transitioning high to low
- c. Clock transitioning low to high
- d. Clock transitioning high to low

2. What is the major difference between SDRAMs and DDR SDRAMs?
- a. DDR SDRAMs have twice the storage density of SDRAMs
- b. DDR SDRAMs accept and provide data at twice the rate of SDRAMs
- c. Operations of DDR SDRAMs are initiated by a low to high clock transition
- d. Twice as many DDR SDRAMs fit on a DIMM

3. In a DDR SDRAM, what circuit is responsible for providing precisely timed internal clock signals?
- a. Clock Buffer
- b. CONTROL LOGIC
- c. DLL
- d. No special circuitry is needed for the DDR SDRAM

4. What is the maximum clock frequency for the Micron 512Mb DDR SDRAM discussed in the course, for speed grade -6 and CAS Latency = 2?
- a. 200 MHz
- b. 166 MHz
- c. 133 MHz
- d. 100 MHz

5. What are the logic states of CS#, RAS#, CAS# and WE# to command a WRITE operation in a DDR SDRAM?
- a. L-H-L-H
- b. L-H-L-L
- c. L-H-H-L
- d. L-L-H-L

6. For READ and WRITE operations, which address input does not provide one of the addresses to select the starting column?
- a. A8
- b. A9
- c. A10
- d. None of the above

7. In an ACTIVE operation, which of the following actions occurs?

○ a. The desired bank is selected
○ b. The desired row is selected
○ c. Sense amplifiers detect and amplify small voltage differences
○ d. The desired starting column is selected
○ e. None of the above
○ f. All of the above
○ g. All of the above except column selection

8. In a READ operation, which of the following actions occurs?
○ a. The desired bank is selected
○ b. The desired starting column is selected
○ c. Data on the I/O lines is amplified
○ d. None of the above
○ e. All of the above

9. For a DDR SDRAM with 8 input/output (DQ) pins, how many columns will provide data during the initial prefetch?
○ a. 4
○ b. 8
○ c. 16
○ d. 32

10. Which bits of the Mode Register in a DDR SDRAM specify the Burst Length?
○ a. Bits 0, 1 and 2
○ b. Bit 3
○ c. Bits 4, 5 and 6
○ d. Bits 7 to n

11. For a x8 DDR SDRAM and a burst length of 4, how many data bits will appear sequentially on each DQ pin?
○ a. 1
○ b. 2
○ c. 4
○ d. 8

12. What is CAS Latency?
○ a. CAS Latency is the time in clock cycles from the registration of the ACTIVE command to the appearance of valid data on the DQ pins.
○ b. CAS Latency is the time in clock cycles from the registration of the READ command to the appearance of valid data on the DQ pins.
○ c. CAS Latency is the time in clock cycles from the registration of the READ command to the registration of the ACTIVE command.

13. If a READ command is registered at Time = T0 and CAS Latency (CL) is 3, when will the first bit of valid date appear on the DQ pins?
○ a. Time = T2
○ b. Time = T2n
○ c. Time = T3
○ d. Time = T4

14. In the Extended Mode Register of a DDR SDRAM, which bit controls drive strength, and what logic level of that bit specifies Normal drive strength?

○ a. Bit 0 = 0
○ b. Bit 0 = 1
○ c. Bit 1 = 0
○ d. Bit 1 = 1

15. Why is a DLL required on a DDR SDRAM?
○ a. Because timing margins on a DDR SDRAM are much tighter than on an SDRAM
○ b. To align the data edges to clock transitions at the end of CAS Latency
○ c. Because on-chip circuit delays vary with processing, temperature and power supply voltage
○ d. None of the above
○ e. All of the above

16. In a DLL, what is the function of the Delay Comparator and Tap Adjust circuit?
○ a. Replicate the delay of circuits in the clock path that are outside of the feedback path
○ b. Provide an adjustable delay to the internal clock signal
○ c. Compare the internal clock to the output of the Delay Model and adjust the Multiplexer tap until those two signals rise simultaneously
○ d. Buffer the external clock signal so it is not loaded by high on-chip capacitance

17. In going from DDR to DDR2 SDRAMs, the most obvious change is the addition of ODT. What does ODT stand for?
○ a. Off-Die Termination
○ b. On-Die Termination
○ c. 0 Delay Time
○ d. Over Dynamic Timing

18. During which operations is ODT normally used?
○ a. READ operations
○ b. WRITE operations
○ c. READ and WRITE operations, but not others
○ d. All operations

19. In the DDR2 Extended Mode Register, if bits 6 and 2 are both set to 1, what value will R_{TT} be set to?
○ a. Infinity
○ b. 75Ω
○ c. 150Ω
○ d. 50Ω

20. In a DDR2 SDRAM, how does the Posted CAS# capability affect the command sequence?
○ a. Posted CAS# allows ACTIVE and READ commands to be issued on successive clock cycles instead of being separated by t_{RCD}(Min)
○ b. Posted CAS# allows two ACTIVE commands to be issued on successive clock cycles
○ c. Posted CAS# allows a READ command to occur immediately before an ACTIVE command
○ d. Posted CAS# diverts the READ command to the next DDR2 SDRAM on the DIMM

21. When using Posted CAS# in a DDR2 SDRAM, the Extended Mode Register stores bits specifying the Additive Latency (AL). Find the minimum value of AL for the following conditions: t_{RCD}(Min) = 15 ns; clock cycle time = 5 ns; READ command is issued immediately after the ACTIVE command.
○ a. 1
○ b. 2

○ c. 3
○ d. 4

22. In a DDR2 SDRAM, assume Additive Latency = 3 and CAS Latency = 5; and that the ACTIVE and READ commands are issued on successive clock cycles. Calculate the READ Latency and the random-access time.
○ a. Read Latency = 5; random access time = 6
○ b. Read Latency = 6; random access time = 7
○ c. Read Latency = 7; random access time = 8
○ d. Read Latency = 8; random access time = 9

23. Which value of CAS Latency is not available in DDR2 SDRAMs?
○ a. 3
○ b. 3.5
○ c. 4
○ d. 5
○ e. 6

24. In DDR3 SDRAMs, what added ODT features are provided?
○ a. Calibration via a precision external resistor
○ b. Selectable output driver impedance
○ c. Dynamic ODT
○ d. None of the above
○ e. All of the above

25. Suppose we want R_{TT} = 120Ω and R_{ON} (Output Drive Strength) = 34Ω. What values must bits 9-6-2 and 5-1 of Mode Register 1 (MR1) be set to?
○ a. Bits 9-6-2 = 1-0-0 and bits 5-1 = 0-0
○ b. Bits 9-6-2 = 0-1-0 and bits 5-1 = 0-1
○ c. Bits 9-6-2 = 1-0-1 and bits 5-1 = 0-1
○ d. Bits 9-6-2 = 0-1-0 and bits 5-1 = 0-0

26. In a DDR3 SDRAM, assume ACTIVE and WRITE commands are issued on successive clock cycles. Also assume CAS Latency = 5; Additive Latency = 6; and CAS Write Latency = 6. Calculate Write Latency (WL).
○ a. 11
○ b. 12
○ c. 13
○ d. 17

27. In a DDR3 SDRAM with 8 DQ pins, how many data bits are prefetched in response to a READ command?
○ a. 8
○ b. 16
○ c. 32
○ d. 64
○ e. 128

28. Which signal integrity methods are included in DDR4 SDRAMs?
○ a. Parity detection
○ b. Cyclic redundancy check (CRC)
○ c. Both of the above
○ d. None or the above

29. In a DDR4 memory device, what is the function of voltage VPP?

- a. To program non-volatile RAM cells in the mode register
- b. To activate the cell-access transistors
- c. To block access to protected areas of memory
- d. To erase selected cells prior to writing them

30. What percentage power savings are anticipated for the DDR4 architecture, versus an equivalent DDR3 memory device?

- a. 10% to 20%
- b. 20% to 30%
- c. 30% to 40%
- d. 40% to 50%

31. What characteristic of memory devices has remained unchanged during the evolution from SDRAM to DDR5 SDRAM?

- a. Data transfer rate
- b. Prefetch width
- c. CAS Latency
- d. DQ Width
- e. Burst length

32. What is the purpose of using redundant rows and columns of memory cells in DRAMs?

- a. To reduce access time by eliminating slow rows or columns
- b. To improve manufacturing yields
- c. To reduce chip size
- d. To save design time
- e. To evaluate new cell designs

33. In the redundancy discussion, how are the fuses programmed?

- a. Laser
- b. High current
- c. EEPROM
- d. Mask

34. Which of the following is not a proper DIMM nomenclature?

- a. PC2100
- b. PC2-8500
- c. PC3200
- d. PC2-3200
- e. PC3-3200