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Continuing Education Course #102
Memories in Computers
Part 1: Overview and DRAM Introduction

1. How much DRAM was in the first IBM PC?
- a. 4Kb
- b. 16Kb
- c. 16KB
- d. 64KB

2. What problem have memory designers been fighting since 1990?
- a. Memory chips are too expensive to gain widespread usage.
- b. Memory chips provide data at too slow a rate to match microprocessors.
- c. Memory chips dissipate too much power, so cooling has become a major problem.
- d. There are so many different and incompatible memory designs that users are confused.

3. What factor received the most attention in memory development up to 1990?
- a. Increased memory density (the number of bits per chip)
- b. Faster memory access times
- c. Smaller memory chip sizes
- d. Reduced memory power consumption

4. What type of memory combines extremely low cost with non-volatility?
- a. DRAM
- b. Flash
- c. Magnetic Hard Drive
- d. SRAM

5. What two types of memories store information in the form of charge on tiny capacitors?
- a. DRAM and SRAM
- b. Hard Drive and DRAM
- c. Flash and SRAM
- d. DRAM and Flash

6. Based on current cost estimates, how much more expensive is non-volatile memory implemented as Flash in a solid-state drive compared to a conventional hard drive?
- a. About 10 times more expensive
- b. About 23 times more expensive
- c. About 52 times more expensive
- d. About 84 times more expensive

7. If SRAM is so expensive, why is it used?

○ a. SRAM has the desirable property of non-volatility.
○ b. SRAM can achieve much higher densities per chip than Flash or DRAM.
○ c. SRAM has much faster random access times than any other type of memory.

8. If Flash is about half the cost of DRAM on a per MB basis, why hasn't Flash replaced DRAM?
○ a. The writing time of Flash chips is much too long for use as temporary storage in a computer.
○ b. Flash chips have not achieved the storage density that DRAMs have.
○ c. Flash chips dissipate too much power when they are in the idle state.

9. In the i1102, what was the structure of the memory cell?
○ a. One transistor and one capacitor
○ b. Three transistors and an inherent capacitor
○ c. Four transistors and two resistors
○ d. Six transistors

10. What causes loss of charge from the capacitor in a 1T-1C cell DRAM?
○ a. Parasitic diodes connected to the top capacitor electrode
○ b. Light-induced charge pairs
○ c. Bit line bounce couples charge from the capacitor
○ d. Access transistor does not turn completely off

11. What happens if a DRAM is not refreshed?
○ a. It loses the information stored in it.
○ b. It turns off.
○ c. It begins to output data at the wrong time.

12. Who is credited with inventing multiplexed addressing in DRAMs?
○ a. Gordon Moore
○ b. Jack Kilby
○ c. R.J. Proebsting
○ d. Bob Noyce
○ e. M.I. Elmasry

13. What was the initial formulation of Moore's Law?
○ a. The number of transistors per square inch of silicon will double each year for the next 10 years.
○ b. The density of memory bits per chip will quadruple every 3 years for the foreseeable future.
○ c. Intel will continue to dominate the microprocessor business until at least 2000.

14. What two factors have contributed the most to the dramatic increase in bit density?
○ a. Simplification of the memory cell from 3 transistors to 1 transistor and 1 capacitor and chip size increase
○ b. Memory cell size reduction and chip size increase
○ c. Chip size increase and stacking two chips in a package
○ d. Package size reduction and power supply voltage reduction

15. How are memory cells arranged on a DRAM chip?
○ a. In a pseudo-random pattern to prevent interaction
○ b. In a circular pattern so all line lengths can all be equal
○ c. In a matrix pattern of rows and columns

16. During a READ cycle of a DRAM, column addresses are provided before row addresses.

- a. True
- b. False

17. In a DRAM, what signal gates in the column addresses?
- a. Clock rising edge
- b. Clock falling edge
- c. CAS/ rising edge
- d. CAS/ falling edge

18. In a DRAM, valid data reaches the DATA OUT pin as soon as the DATA OUT Amp supplies it.
- a. True
- b. False

19. What factor is common to all of the accelerated access modes of a DRAM?
- a. CAS/ must cycle to obtain a new column address.
- b. The new column address must be provided by the system.
- c. An address transition detector tells the DRAM when a new column address has been provided.
- d. All data bits must come from the row of memory that was initially accessed.

20. What is the meaning of “fill frequency”?
- a. Fill frequency indicates how fast a memory can supply the first 8 bits (byte) of information.
- b. Fill frequency is a measure of how much charge is stored during the write of a “1” to a memory cell.
- c. Fill frequency describes how fast all of the bits in a memory can be read or written.
- d. Fill frequency is the frequency of the system clock.

21. Which one of the following memories would have the highest fill frequency, assuming all have the same access and cycle times?
- a. 128M words x 1 bit
- b. 64M words by 2 bits
- c. 32M words x 4 bits
- d. 16M words x 8 bits

22. What major feature was added to the DRAM architecture to obtain the SDRAM architecture?
- a. Command inputs
- b. Clock input
- c. Command decoder
- d. Mode register
- e. All of the above

23. How is an operation initiated in an SDRAM?
- a. RAS/ going low
- b. CAS/ going low
- c. Clock going low
- d. Clock going high

24. Where is the information stored that instructs the SDRAM how many bits of data to output sequentially?
- a. In the system memory controller
- b. In the hard drive
- c. In the SDRAM mode register
- d. In the SRAM cache memory

25. What are the logic states of the command inputs (CS/, RAS/, CAS/ and WE/) to initiate a WRITE operation?
- a. L-H-L-H
- b. L-H-L-L
- c. L-L-H-L
- d. L-L-L-L

26. In an SDRAM, as soon as data is amplified by the DATA OUT AMP, it is immediately sent to the DATA OUT pin.
- a. True
- b. False

27. In an SDRAM, what is the meaning of CAS Latency?
- a. CAS Latency is the delay in clock cycles between the ACTIVE command and the READ command.
- b. CAS Latency is the delay in clock cycles between the ACTIVE command and the availability of the output data.
- c. CAS Latency is the delay in clock cycles between the READ command and the availability of the output data.

28. When considering access time in an SDRAM, the access time from the READ command (CAS access time) is the CAS Latency multiplied by the clock cycle time.
- a. True
- b. False

29. How is the random access time of an SDRAM calculated?
- a. It is equal to the CAS access time.
- b. It is the sum of CAS access time and the minimum value of ACTIVE to READ command delay, tRCD.
- c. It is the minimum value of ACTIVE to READ command delay, tRCD, minus the CAS access time.

30. In Data Burst operation in an SDRAM, how is the column address changed?
- a. It is changed each time the Clock rises from low to high.
- b. It is changed each time CAS/ cycles from high to low.
- c. An ATD circuit detects an external change in address and conveys it to the SDRAM column select circuitry.
- d. A strobe signal from the system indicates that the data bit has been received, thus telling the SDRAM to advance to the next column address.

31. How many data bits are output by each READ operation of an SDRAM with 8 DQ pins and a burst length of 2?
- a. 8
- b. 16
- c. 32
- d. 64

32. Which bits in the Mode Register are used to store CAS Latency information?
- a. Bits 0, 1 and 2.
- b. Bit 3.
- c. Bits 4, 5 and 6.
- d. Bits 7 and 8.
- e. Bit 9.
- f. Bits 10, 11 and 12.

33. What organization has been primarily responsible for providing memory standards?
- a. IEEE
- b. Intel
- c. JEDEC JC-42

- ○ d. Micron
- ○ e. Texas Instruments