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Continuing Education Course #083
Phase Lock Loops

1. The Voltage Controlled Oscillator is modeled as :
- a. a Gain Stage,
- b. a Differentiator
- c. an Integrator.

2. The Loop filter in the PLL discussed adds an integrator to the loop:
- a. True,
- b. False.

3. The Loop filter in the PLL discussed adds a “zero” to the loop:
- a. True,
- b. False.

4. The Loop filter in the PLL discussed adds a “pole” to the loop:
- a. True,
- b. False.

5. Multiplication of sinusoids is a linear operation with a transfer function description:
- a. True,
- b. False.

6. FSK modulation produces VCO sidebands:
- a. True,
- b. False.

7. A Costas Loop can be used for Carrier synchronization of a Bi-Phase modulated signal
- a. True,
- b. False.

8. A Costas Double Loop can be used for Carrier synchronization of a Bi-Phase modulated signal
- a. True,
- b. False.

9. A Costas Double Loop can be used for Carrier synchronization of a QPSK modulated signal
- a. True,
- b. False.

10. A Costas Double Loop used for Carrier synchronization of a QPSK modulated signal does not have any polarity uncertainties
- a. True,
- b. False.

11. The analog multiplication of a sine by a cosine wave signal produces a result at the sum of the individual frequencies:

○ a. True,
○ b. False.

12. Frequency synthesis can employ a digital PLL:

○ a. True,
○ b. False.

13. The “Exclusive-OR” phase detector behavior depends on the waveform duty-cycle:

○ a. True,
○ b. False.

14. The Phase-Frequency Detector (PFD) is an Asynchronous Logic circuit:

○ a. True,
○ b. False.

15. The Phase-Frequency Detector (PFD), in each cycle, produces

○ a. a PU pulse
○ b. a PD pulse
○ c. both PU and PD pulses

16. The Sink-Source-Float (SSF) is a Charge-Pump circuit:

○ a. True,
○ b. False.

17. The Sink-Source-Float (SSF) is used with an Impedance to perform loop filter functions:

○ a. True,
○ b. False.

18. PLL sampling introduces a Nyquist “notch” in the feedback loop:

○ a. True,
○ b. False.

19. PLL sampling introduces a delay in the feedback loop:

○ a. True,
○ b. False.

20. The digital PLL does not require a loop filter:

○ a. True,
○ b. False.

21. The Sink-Source-Float (SSF) produces spurious responses due to its sampling :

○ a. True,
○ b. False.

22. Spurious signals in a digital frequency synthesizer are greater for large values of “N”:

○ a. True,
○ b. False.

23. Fractional-N frequency synthesis can be used to decrease spurious signals:

○ a. True,
○ b. False.

24. First-order Δ -Σ loops are preferred to avoid “tone” production by the Δ -Σ :

- a. True,
- b. False.

25. Digital communication technology supports error free communication under some circumstances.:

- a. True,
- b. False.