*A SunCam online continuing education course*

# Phase Lock Loops©

**By**

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## 1.0 Phase Lock Loop Introduction

This course develops the Phase-Lock Loop (PLL) with considerations from classical feedback theory to produce a simple analog loop for demonstration purposes.

We analyze the components, linearizing them as required and show the second-order nature of the loop with the PZ compensation filter for stability.

We demonstrate the PLL capability as a Frequency-Shift Keyed (FSK) receiver demodulator for a Frequency-Modulated (FM) signal.

We introduce the Costas Loop variant of the PLL for double-sideband, suppressed-carrier synchronization using a Bi-Phase modulated signal. We introduce the "Double-Loop" variant of the Costas Loop, showing the equivalence of the saturated signal paths for the Bi-Phase modulation in a summing loop, and the requirements for a difference term for Quadri-Phase Shift Keyed (QPSK) signals. We discuss and demonstrate the $180^{o}$ phase uncertainty associated with the receiver synchronization.

We introduce the digital PLL for frequency synthesis applications, demonstrating the relationships between loop bandwidth and channel spacing. We illustrate the use of the "Exclusive-OR" logic function as a phase detector and show the advantage of the Phase-Frequency Detector (PFD) and Sink-Source-Float (SSF) implementations.

We develop the stability requirements for the components and the design of a PZ compensator for the digital PLL, including the use of a transconductance and impedance for loop filter application.

We discuss the effects of the sampling delay on the magnitude and phase characteristics of the loop.

We demonstrate the time and frequency domain performance of a macro-model using the parameters and show that the discrete-time performance is well predicted, but that there are noise effects from the PU/PD pulses in the PFD.

We introduce the Fractional-N synthesis technique and contrast the averaging and $\Delta$–$\Sigma$ modulator approaches to the oversampling used in the Fractional-N approach.

  

## 2.0 Classical Feedback Control System: Open Loop Parameters for Stability

The basic model for a feedback control system is shown in figure 2.0 below, and consists of the system block ***G***, the feedback block ***H***, and the summation (difference) block ***Σ***, with the signals as labeled.

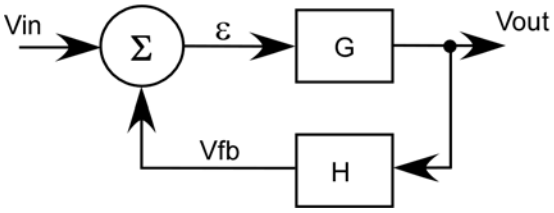


**Figure 2.0 Classical Feedback Control System Block Diagram**

We use Laplace notation in the following to describe the system as follows:

$$\frac{V_{out}}{\varepsilon} = G(s) \qquad [2.0]$$

$$\frac{V_{fb}}{V_{out}} = H(s) \qquad [2.1]$$

$$\varepsilon = V_{in} - V_{fb} \qquad [2.2]$$

We solve for the closed loop equation as follows:

$$\frac{V_{out}}{G(s)} = V_{in} - H(s)V_{out} \qquad [2.3]$$

$$V_{out} = G(s)V_{in} - G(s)H(s)V_{out} \qquad [2.4]$$

$$[1 + G(s)H(s)]V_{out} = G(s)V_{in} \qquad [2.5]$$

$$\frac{V_{out}}{V_{in}} = \frac{G(s)}{1 + G(s)H(s)} \qquad [2.6]$$

  

Underlying the classical description of equation [2.6} are the assumptions that the system components are Linear, Time-Invariant (LTI) so that the mathematics are appropriate to the development of the transfer function.

We will use the block diagram and basic concepts of feedback control, but ignore some underlying requirements for the initial development of the Phase Lock Loop (PLL) concepts. We begin using the PLL Block Diagram in figure 2.1 below.

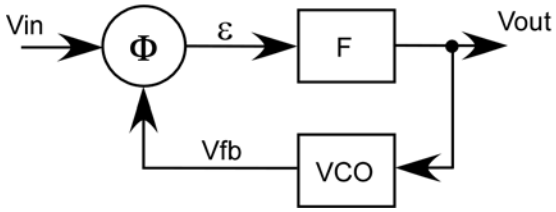


**Figure 2.1 PLL System Block Diagram**

In figure 2.1 above, we have substituted the Phase Detector denoted as ***Φ*** for the ***Σ*** summation block in the classical feedback control system. The substitution is reasonable to the first order because the phase detector produces a signal proportional to the phase difference at its inputs. It, however, may only be linear over a restricted range of inputs as we shall explore later. The Loop-Filter denoted as ***F*** may be an LTI implementation, but may have much more complex behavior in some applications. The Voltage-Controlled Oscillator ***VCO*** can be linear as a source of "Phase" over a range of operation, and we will assume that we meet the requirements for now.

We explore the LTI requirements by using a multiplier for the phase detector in one form of PLL and argue that the clearly non-linear product of signals can be considered linear under certain conditions. Let us define:

$$V_{in} = A_{in}\cos\varpi_0 t \qquad [2.7]$$

$$V_{fb} = A_{fb}\sin\left[\left(\varpi_0 + \varpi_{err}\right)t + \phi\right] \qquad [2.8]$$

In a multiplication of the two signals, we employ the trigonometric identity:

$$\sin\alpha\cos\beta = \frac{1}{2}\sin\left(\alpha-\beta\right)+\frac{1}{2}\sin\left(\alpha+\beta\right) \qquad [2.9]$$

  

$$\varepsilon(t) = A_{fb}\sin\left[(\varpi_0 + \varpi_{err})t + \phi\right] \bullet A_{in}\cos(\varpi_0)t \qquad [2.10]$$

$$\varepsilon(t) = A_{in}A_{fb}\left[\frac{1}{2}\sin(\varpi_{err}t + \phi) + \frac{1}{2}\sin((2\varpi_0 + \varpi_{err})t + \phi)\right] \qquad [2.11]$$

$$\varepsilon(t) = \frac{A_{in}A_{fb}}{2}\sin(\varpi_{err}t + \phi) + \frac{A_{in}A_{fb}}{2}\sin((2\varpi_0 + \varpi_{err})t + \phi) \qquad [2.12]$$

If we assume that the term:

$$\frac{A_{in}A_{fb}}{2}\sin((2\varpi_0 + \varpi_{err})t + \phi) \qquad [2.13]$$

is "rejected" by the loop filter ***F***, we are left with:

$$\varepsilon(t) = \frac{A_{in}A_{fb}}{2}\sin(\varpi_{err}t + \phi) \qquad [2.14]$$

Under conditions that we shall define as "locked," then $\omega_{err} = 0$, and

$$\varepsilon(t) = \frac{A_{in}A_{fb}}{2}\sin(\phi) \qquad [2.15]$$

Using the series expansion for the sin, we have:

$$\varepsilon(t) = \frac{A_{in}A_{fb}}{2}\left[\phi - \frac{\phi^3}{3!} + \frac{\phi^5}{5!} - \frac{\phi^7}{7!}\bullet\bullet\bullet\right] \qquad [2.16]$$

We can find a "locked" condition with a range of values for $\phi$ that we can consider "linear" around $\phi = 0$. The conditions we have imposed permit a small-signal region of linearity around a solution point in a locked condition, and we will depend on the feedback behavior of the non-linear to allow us to approach sufficiently close to this point to "acquire" a locked condition. We treat the scaling constant with dimension of volts per radian as follows:

$$\frac{A_{in}A_{fb}}{2} = K_{\phi} \qquad [2.17]$$

The ***VCO*** is treated as a source of "Phase" by defining it as an integral. We define it with its own scaling constant in equation [2.18] below.

  

$$\phi_{VCO} = \frac{K_{VCO}}{s} \qquad [2.18]$$

The constant ***KVCO*** is the characteristic of the VCO that defines the "gain" as Hertz/Volt (or radians per Volt, if that is your preference). Using the classical feedback control block diagram, we can define our small-signal, locked condition, loop performance as follows:

$$\frac{V_{out}}{V_{in}} = \frac{K_\phi F(s)}{1 + F(s)\dfrac{K_{VCO}K_\phi}{s}} \qquad [2.19]$$

The "open-loop" behavior is defined by the product defined as ***T(s)*** in equation [2.19] below and is subject to all the constraints associated with feedback control of an integrator.

$$T(s) = F(s)\frac{K_{VCO}K_\phi}{s} \qquad [2.20]$$

We have already inferred above that the ***F(s)*** will be required to prevent a high frequency term from the phase detector from propagating, and therefore it must have at least one pole in its transfer function. Typically, with the simple example loop we are developing, we would employ a pole-zero compensator in the ***F(s)*** function for reasons that will become apparent as the example develops.

$$F(s) = \frac{K_F}{s}\left(\frac{\tau_z s + 1}{\tau_P s + 1}\right) \qquad [2.21]$$

$$T(s) = K_\phi \frac{K_F}{s}\left(\frac{\tau_z s + 1}{\tau_P s + 1}\right)\frac{K_{VCO}}{s} = \frac{K_{VCO}K_\phi}{s} \bullet \frac{K_F}{s}\left(\frac{\tau_z s + 1}{\tau_P s + 1}\right) \qquad [2.22]$$

With the ***F(s)*** function we have chosen, the small-signal, open-loop ***T(s)*** becomes a double integrator with a "Lead-Lag" or pole-zero compensator. For purposes of illustration, we group the terms to show the single integrator that we are required to compensate, add the compensator characteristics and review the composite open loop characteristics in the following.

  

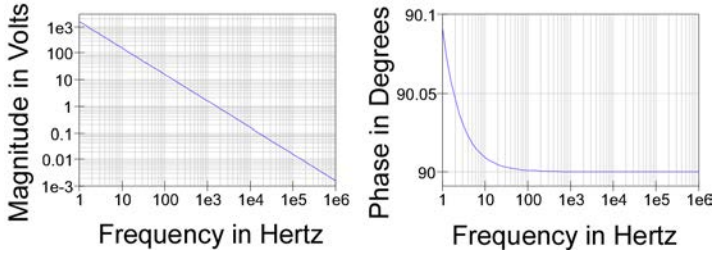


**Figure 2.2 PLL Un-Compensated Open Loop**

In figure 2.2 above and equation [2.23] below, we show the Bode Plot and mathematical model of the VCO followed by the phase detector combined in the open-loop model. The Bode plot reflects an intercept with $s = K_\phi K_{VCO} = 2\pi f$, with $f$ = 1600 Hz.

$$K_\phi \phi_{VCO}(s) = \frac{K_\phi K_{VCO}}{s} \qquad [2.23]$$

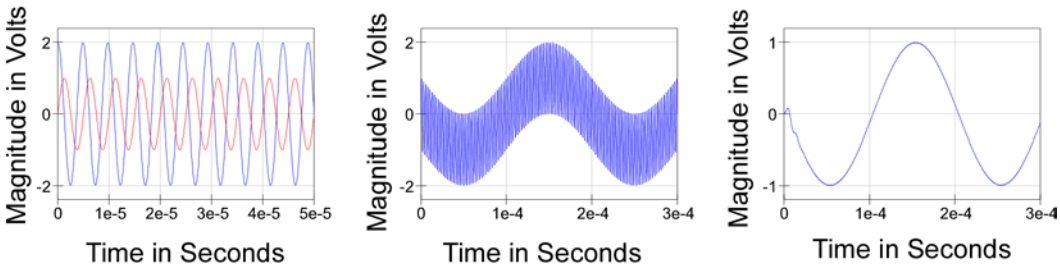


**Figure 2.3 Phase Detector: *VCO*, *Vin*, VCOxVin Product, and Lowpass Output**

In figure 2.2 above, we show the ***VCO*** sine wave in blue and the $V_{in}$ sine wave in red. The ***VCO*** signal is 2 Volts peak at 205 kHertz and the $V_{in}$ sine wave is 1 Volt peak at 200 kHertz, so that the difference frequency is 5 kHertz. The phase detector is implemented as a multiplier as given in equation [2.12] and the product provides sum and difference frequencies, each with $A_{in}A_{fb}/2$ = 1x2/2 = 1 Volt peak sine wave shapes. We see the product in the center of the illustration with the two components superimposed. Finally, we see the difference frequency alone, with the high frequency component filtered from its waveform.

We note that the ***VCO*** sine wave is a cosine waveform at the initial time, being at its peak value, while the $V_{in}$ sine wave is a sine waveform being at zero at the initial time. True to the product of the ***sin* x *cos***, the resulting product shown is a sine waveform with an initial value of zero. The difference frequency is rotating through its 2π radian circle at a 5 kHertz rate.

  

We can say that the purpose of the PLL feedback loop is to reduce the frequency difference to zero, and in the interim, the phase detector provides a voltage proportional to the instantaneous phase difference between the $V_{in}$ sine wave and the feedback-controlled ***VCO*** sine wave.

Given that the phase detector provides the difference as:

$$V_{\phi}(t) = \frac{A_{in}A_{fb}}{2}\sin(\phi(t)) = 1 \bullet \sin(\phi(t)) \qquad [2.24]$$

We find the slope, or gain as:

$$K_{\phi} = \left.\frac{dV_{\phi}(t)}{d\phi}\right|_{t=0} = 1 \bullet \left.\frac{d\sin(\phi(t))}{d\phi}\right|_{t=0} = 1 \bullet \cos(0) = 1 \qquad [2.25]$$

Thus, we know that $K_{\phi} = 1$ V/radian and have parameterized the phase detector.

We deal with the VCO in a similar fashion, knowing that $K_{\phi}K_{VCO} = 2\pi f$, with $f = 1600$ Hz.

$$K_{VCO} = 2\pi\frac{1600 radians}{V} \qquad [2.26]$$

We have chosen to implement the VCO with a nominal plus control voltage architecture. We have the nominal frequency set at 200 kHz and an incremental variation that provides the KVCO gain as a superposition added to the nominal center frequency. We use a replica of the VCO as a signal source for Frequency-Shift-Keyed (FSK) signaling to show the acquisition of a lock condition, as well as a tracking of the FSK source.

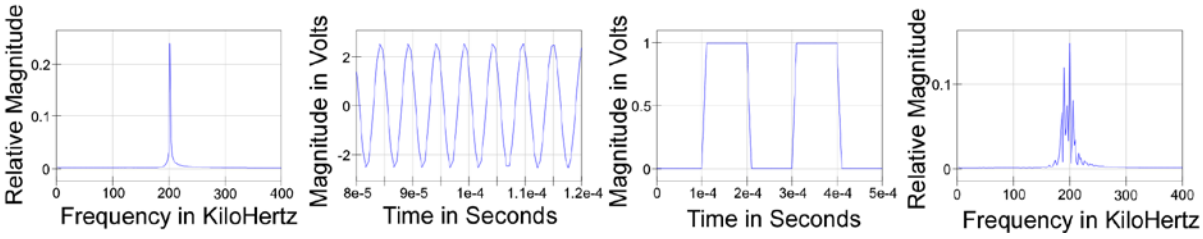


**Figure 2.4 PLL VCO Nominal Spectrum, Wave Shape, FSK Modulation and Spectrum**

We see in figure 2.4 above that the VCO has a single spectral line at 200 kHertz until it is modulated. With the application of a 50 kHertz square wave to the frequency control input, the VCO shifts to produce spectral lines with 1.6 kHertz line spacing.

  

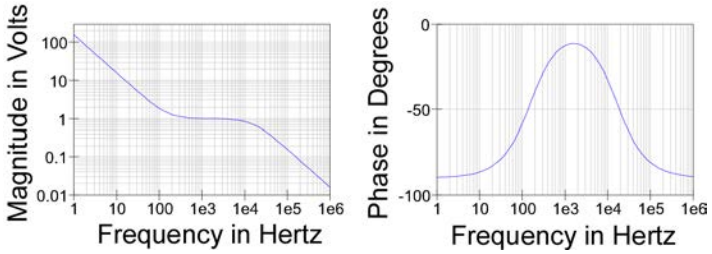


**Figure 2.5 PLL PZ Compensator**

We introduce the Pole-Zero (PX) compensator shown in figure 2.5 into the loop, completing the open-loop block sequence of connections. The parameters of the PZ compensator shown above include $K_F = 10^{-3}$, $\tau_Z = 10^{-3}$, and $\tau_Z = 10^{-5}$.

$$F(s) = \frac{10^{-3}}{s}\left(\frac{10^{-3}s+1}{10^{-5}s+1}\right) \qquad [2.27]$$

We see that adding the compensator of figure 2.5 to the open-loop VCO/Phase detector combination of figure 2.2, we produce the compensated open-loop characteristic shown in figure 2.6 below.

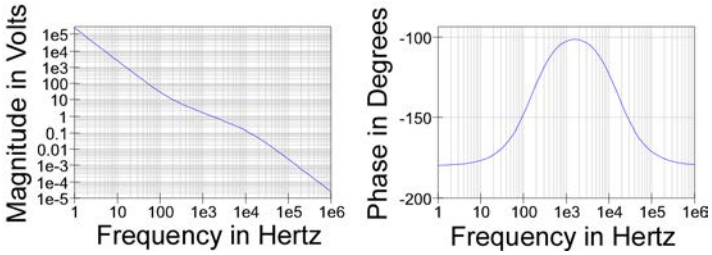


**Figure 2.6 PLL Compensated Open Loop**

Most notable of the effects of the PZ compensation are the double integrator characteristic below 100 Hertz indicated by the two-decade magnitude decrease per decade of frequency increase, the change of slope between ~200 Hertz and ~10 kHertz to one decade per decade with the phase margin increase at the unity gain frequency of ~2 kHertz to about 80° for good stability, and a return to a greater magnitude slope at higher frequencies to help alleviate the higher frequency components produced by the phase detector "sum" terms.

  

### 3.0 Classical Feedback Control System: PLL Closed Loop Behaviors

The ***PLL*** is often employed as the detector for an FM modulated signal, and in figure 3.0 below, we show it in that context for closed-loop discussions.

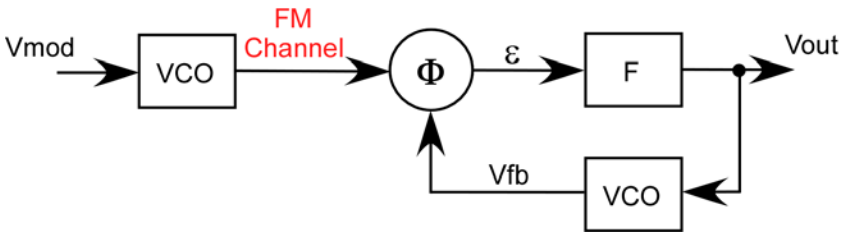


**Figure 3.0 Closed Loop PLL Used as FM Demodulator**

In figure 3.0 above, we added a duplicate copy of the ***VCO*** structure to produce the FM modulated signal for the FM Channel. In figure 3.1 below, we show the PLL acquiring a lock onto a 1V un-modulated FM Channel replica signal at 200 kHertz.

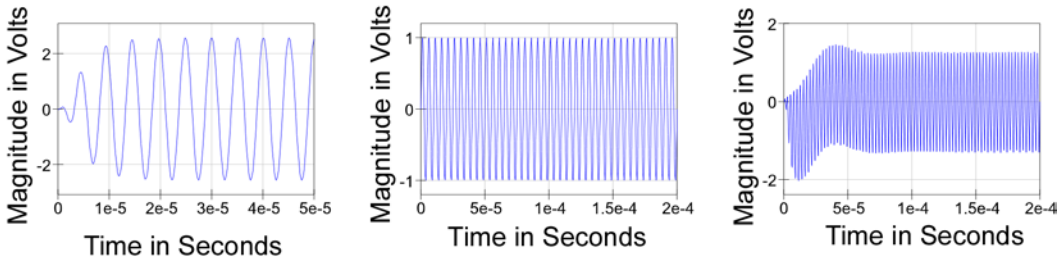


**Figure 3.1 PLL Compensated Open Loop Acquiring Lock to a Static Reference**

In figure 3.1 above, we see that the VCO inside the PLL loop in the leftmost panel, starts from a zero-Volt initial condition, and as soon as the loop is started, it begins oscillation at nearly 200 kHertz. The VCO only takes about 3 cycles to reach to reach ~2V peak sinusoidal steady-state oscillation condition. We have chosen a 1V peak, 200 kHertz signal in the center panel of figure 3.1, to represent the FM channel signal, and see that the phase-detector, as shown in the rightmost panel indicates a sinusoidal signal at a higher frequency than the reference as expected, as well as a superimposed  low-frequency, difference-frequency term with near static results.

We show in figure 3.2 below in the leftmost panel, the output signal from the PZ compensator, with the higher frequency sum-frequency terms suppressed relative to the low frequency difference frequency. In the center panel, we added an external lowpass filter to

  

fully suppress the sum-frequency terms, but we cannot include it within the loop without disturbing the carefully constructed loop phase-margin. The filtered signal is, however, indicative of the feedback to the VCO that completes the closed loop. In the rightmost panel of figure 3.2 below, we include the sum of the $V_{out}$ signal plus the static bias signal that determines the ***VCO*** frequency. We see the $V_{out}$ signal contribution as a small negative-going perturbation on the VCO control signal, and reveals that ~1V at the VCO implies 200 kHertz center-frequency operation while the ~0.5 V signal from the PZ compensator is attenuated, inverted, and added to the bias to provide the correct ~1.6 kHertz/Volt $K_{VCO}$ gain constant.

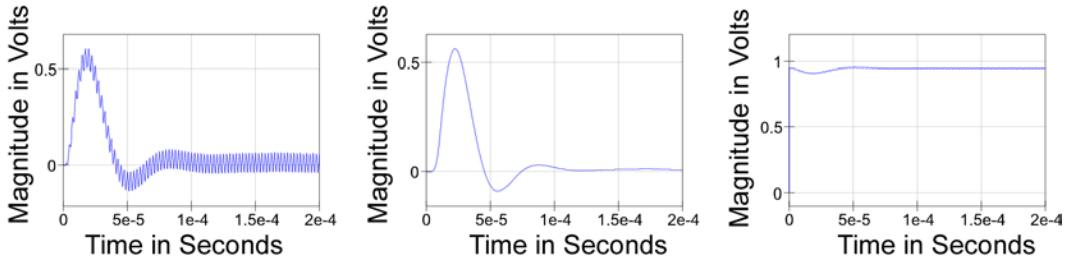


**Figure 3.2 PLL Compensated Closed Loop Lock Acquisition**

In figure 3.2 above, we have demonstrated that the parameterization developed in the prior section supports a stable locked condition for the ***PLL***, as well as sufficient feedback to support acquisition of the "locked" condition following a startup. In figure 3.3 below, we include the same ***PLL*** structure, but with the replica VCO modulated by the FSK modulation shown in figure 2.4 of the prior section.

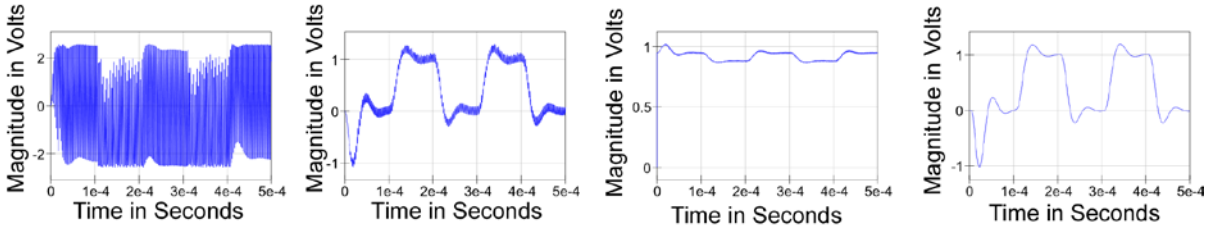


**Figure 3.3 PLL Compensated Closed Loop Lock Acquisition and FSK Demodulation**

In figure 3.3 above, we have introduced the signal from a replica VCO that is FSK modulated. The replica VCO is identical to that employed within the ***PLL*** and has a similar startup transient, but a different starting phase from the 1V peak signal used in figure 3.1 above. In addition, both VCO replicas reach ~2V peak sinusoidal steady-state oscillation condition, as shown by the larger phase detector signal shown in the leftmost panel of figure

  

3.3 above. The next panel shows the ***PLL*** PZ filter feedback to the ***PLL*** VCO, and the next panel shows the ***PLL*** control signal with the square-wave perturbation from the nominal 1V bias condition. The rightmost panel of figure 3.3 shows the externally lowpass filtered version that we could use for FSK demodulation.

**4.0 Suppressed Carrier Communications Application of the PLL**

We have demonstrated the ***PLL*** is employed as the detector for an FSK signal and in the process identified its use for establishing a frequency relationship in the receiver that is equal to that of the transmitter. In many communications scenarios, establishing a synchronizing frequency relationship is an important function in itself. Whenever one side of the communication must be low power, portable, and small, relative to the transmitter, it is useful to synchronize clocking functions in the receiver to the transmitter so that a precise timing generator need not be included in the receiver, but only in the transmitter. In other applications, we will find that there may be physical considerations that cause a frequency shift, such as a Doppler effect that makes tracking the source important, too.

One important application of ***PLL*** technology is establishing a frequency and phase relationship in the receiver despite the lack of a synchronizing frequency component at all. One such case occurs in variants of double-sideband, suppressed-carrier communication links, with the restoration of the "missing" or suppressed carrier frequency.

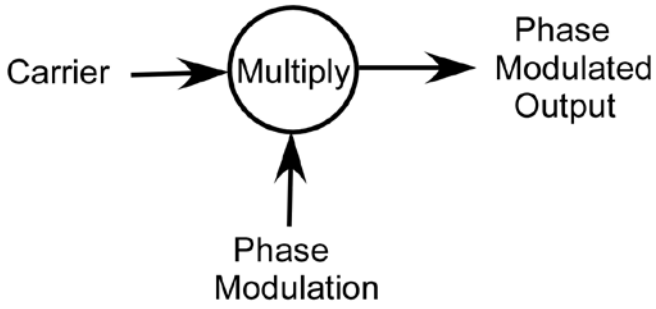


**Figure 4.0 Multiply as a Phase Modulator**

In figure 4.0 above, we show the use of a multiplier as a phase modulator, with the "Phase Modulation" signal restricted to a unit magnitude value with only a polarity change. The polarity change is equivalent to a $180^{o}$ phase shift, and is often called a Bi-Phase modulator. This is one of the simplest of the suppressed-carrier, double sideband modulators.

  

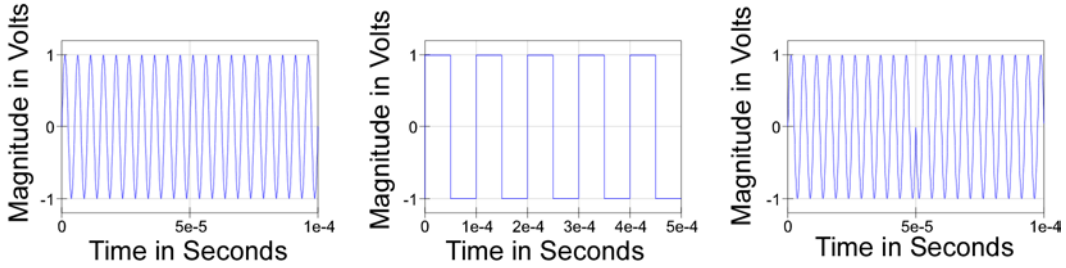


**Figure 4.1 Phase Modulator Wave Forms: Carrier, Modulation, and Product**

In figure 4.1 above, we show the wave forms of the signals applied to the Bi-Phase modulator of figure 4.0, with a 200 kHertz sinusoidal carrier, a 10 kHertz square wave modulation, and the product showing the first phase reversal at the 50 μsec time mark.

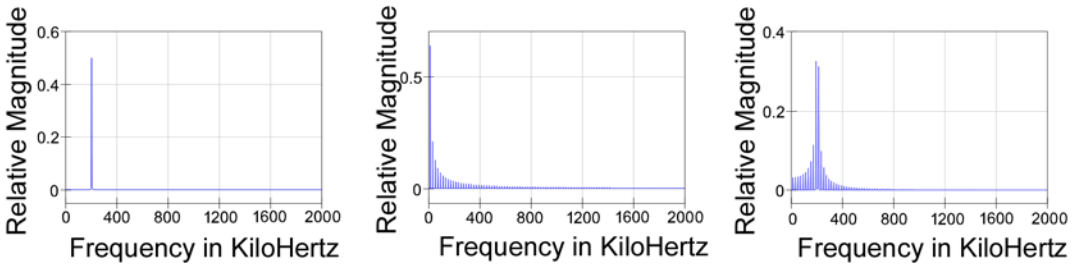


**Figure 4.2 Phase Modulator Spectra: Carrier, Modulation, and Product**

In figure 4.2 above, we show the spectra of the signals applied to the Bi-Phase modulator of figure 4.0, with the pure-tone carrier, the square wave spectra near base band, and the double-sided spectrum of the modulated output waveform. We express the carrier as the sine wave formula in equation [4.0] below, and the square wave as the Fourier series formula in equation [4.1] below, as follows:

$$V_{Carrier} = 1V \bullet \sin 2\pi\left(2 \bullet 10^{5}\right)t \qquad [4.0]$$

$$V_{Mod} = 1V\left[\sin 2\pi\left(1 \bullet 10^{4}\right)t + \frac{\sin 2\pi\left(3 \bullet 10^{4}\right)t}{3} + \frac{\sin 2\pi\left(5 \bullet 10^{4}\right)t}{5} + \bullet\bullet\bullet\right] \qquad [4.1]$$

We expand the product as follows:

$$V_{Carrier}V_{Mod} = \sin 4\pi \bullet 10^{5}t\left[\sin 2\pi \bullet 10^{4}t + \frac{\sin 6\pi \bullet 10^{4}t}{3} + \frac{\sin 10\pi \bullet 10^{4}t}{5} + \bullet\bullet\bullet\right] \qquad [4.2]$$

  

$$V_{Carrier}V_{Mod} = \sin 4\pi \bullet 10^5 t \bullet \sin 2\pi \bullet 10^4 t + \sin 4\pi \bullet 10^5 t \bullet \frac{\sin 6\pi \bullet 10^4 t}{3} + \sin 4\pi \bullet 10^5 t \bullet \frac{\sin 10\pi \bullet 10^4 t}{5} + \bullet\bullet\bullet \quad [4.3]$$

To simplify, we employ the following trigonometric identity:

$$\sin\alpha \sin\beta = \frac{\cos(\alpha-\beta)}{2} - \frac{\cos(\alpha+\beta)}{2} \quad [4.4]$$

We can express the $\boldsymbol{V_{Carrier}}$ and $\boldsymbol{V_{Mod}}$ product as:

$$V_{Carrier}V_{Mod} = \frac{\cos 2\pi\left(2\bullet 10^5 - 10^4\right)t - \cos 2\pi\left(2\bullet 10^5 + 10^4\right)t}{2} + \frac{\cos 2\pi\left(2\bullet 10^5 - 3\bullet 10^4\right)t - \cos 2\pi\left(2\bullet 10^5 + 3\bullet 10^4\right)t}{6} + \frac{\cos 2\pi\left(2\bullet 10^5 - 5\bullet 10^4\right)t - \cos 2\pi\left(2\bullet 10^5 + 5\bullet 10^4\right)t}{10} + \bullet\bullet\bullet \quad [4.5]$$

$$V_{Carrier}V_{Mod} = \frac{\cos 2\pi\left(1.9\bullet 10^5\right)t - \cos 2\pi\left(2.1\bullet 10^5\right)t}{2} + \frac{\cos 2\pi\left(1.7\bullet 10^5\right)t - \cos 2\pi\left(2.3\bullet 10^5\right)t}{6} + \frac{\cos 2\pi\left(1.5\bullet 10^5\right)t - \cos 2\pi\left(2.5\bullet 10^5\right)t}{10} + \bullet\bullet\bullet \quad [4.6]$$

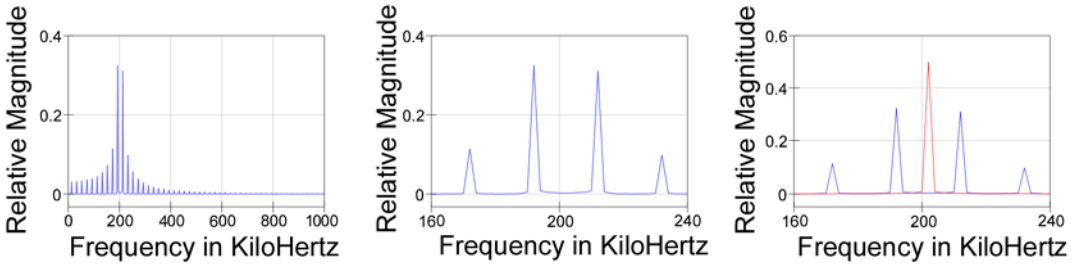


**Figure 4.3 Phase Modulator Spectra: Product Details, expanded, and with Carrier**

In figure 4.3 above, we show the detail spectra of the signals produced by the Bi-Phase modulator, especially, the suppressed carrier nature in the center panel. The rightmost panel

  

shows that same product with the carrier superimposed for reference; it is not really a part of the signal, but included to show it in relation to the upper and lower sidebands produced by the modulation. The particular modulation waveform has no DC component, and any such DC component would produce a spectrum line at the 200 kHertz carrier frequency. Many coded digital waveforms are used that intentionally have no DC component and thus produce a true suppressed carrier as we have shown.

To recover a carrier signal, we employ a variant of the PLL known as the Costas Loop [Costas, J.P., "Synchronous Communications," Proceedings of the IRE, 44, pp 1713-1718, December, 1956], a PLL system that multiplies sidebands to generate a signal at twice the carrier frequency as follows:

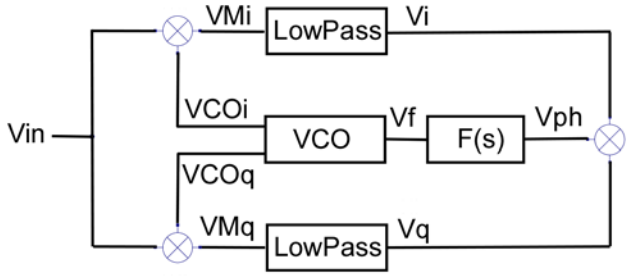


**Figure 4.4 Costas PLL for Double Sideband, Suppressed Carrier Recovery**

The Costas loop employs a ***VCO*** that provides its two outputs in a quadrature or 90$^o$ phase relationship to each other. We employ the trigonometric identities shown in equation [4.7]. and [4.8], and distribute as follows:

$$\cos\alpha\cos\beta = \frac{\cos(\alpha-\beta)}{2} + \frac{\cos(\alpha+\beta)}{2} \qquad [4.7]$$

$$\sin\alpha\cos\beta = \frac{\sin(\alpha-\beta)}{2} + \frac{\sin(\alpha+\beta)}{2} \qquad [4.8]$$

We define the following angular relationships:

$$V_{in} = A[\cos(\varpi_0 - \varpi_{Data})t - \cos(\varpi_0 + \varpi_{Data})t] = A[\cos\beta_- - \cos\beta_+] \qquad [4.9]$$

$$V_{VCOi} = B\cos(\varpi_1 t + \theta_{err}) = B\cos\alpha \qquad [4.10]$$

$$V_{VCOq} = B\sin(\varpi_1 t + \theta_{err}) = B\sin\alpha \qquad [4.11]$$

  

We have the intention of using the PLL feedback behavior to reduce the frequency difference between $\omega_0$ and $\omega_1$ to zero, controlling the $\omega_1$ frequency produced by the quadrature ***VCO*** as the following derivations will show.

$$VM_i = AB\cos\alpha\left[\cos\beta_- - \cos\beta_+\right] = \frac{AB}{2}\left[\cos\alpha\cos\beta_- - \cos\alpha\cos\beta_+\right] \quad [4.12]$$

$$VM_q = AB\sin\alpha\left[\cos\beta_- - \cos\beta_+\right] = \frac{AB}{2}\left[\sin\alpha\cos\beta_- - \sin\alpha\cos\beta_+\right] \quad [4.13]$$

$$VM_i = \frac{AB}{4}\left[\left(\cos(\alpha-\beta_-)+\cos(\alpha+\beta_-)\right)-\left(\cos(\alpha-\beta_+)+\cos(\alpha+\beta_+)\right)\right] \quad [4.14]$$

$$VM_q = \frac{AB}{4}\left[\left(\sin(\alpha-\beta_-)+\sin(\alpha+\beta_-)\right)-\left(\sin(\alpha-\beta_+)+\sin(\alpha+\beta_+)\right)\right] \quad [4.15]$$

With the ***VCO*** frequency "in the neighborhood" of the $V_{in}$ frequency, we configure the Lowpass filters to pass the difference terms and suppress the higher frequency terms, as follows:

$$V_i = \frac{AB}{4}\left[\cos(\alpha-\beta_-)-\cos(\alpha-\beta_+)\right] \quad [4.16]$$

$$V_q = \frac{AB}{4}\left[\sin(\alpha-\beta_-)-\sin(\alpha-\beta_+)\right] \quad [4.17]$$

We produce another multiplier product to generate the $V_{ph}$ signal as the product of $V_i$ times $V_q$ as follows:

$$V_i \bullet V_q = \left(\frac{AB}{4}\right)^2\left[\cos(\alpha-\beta_-)-\cos(\alpha-\beta_+)\right]\bullet\left[\sin(\alpha-\beta_-)-\sin(\alpha-\beta_+)\right] \quad [4.18]$$

We distribute the two terms of the second factor as follows:

$$V_i \bullet V_q = \left(\frac{AB}{2}\right)^2\sin(\alpha-\beta_-)\left[\cos(\alpha-\beta_-)-\cos(\alpha-\beta_+)\right] - \left(\frac{AB}{2}\right)^2\sin(\alpha-\beta_+)\left[\cos(\alpha-\beta_-)-\cos(\alpha-\beta_+)\right] \quad [4.19]$$

  

We distribute the remaining terms to make all four products, as follows:

$$V_i \bullet V_q = \left(\frac{AB}{2}\right)^2 [\sin(\alpha-\beta_-)\cos(\alpha-\beta_-)] - \left(\frac{AB}{2}\right)^2 [\sin(\alpha-\beta_-)\cos(\alpha-\beta_+)] - \left(\frac{AB}{2}\right)^2 [\sin(\alpha-\beta_+)\cos(\alpha-\beta_-)] + \left(\frac{AB}{2}\right)^2 [\sin(\alpha-\beta_+)\cos(\alpha-\beta_+)] \quad [4.20]$$

We apply equation [4.8] to each of the four trigonometric terms as follows:

$$V_i \bullet V_q = \left(\frac{AB}{2}\right)^2 \left[\frac{\sin\{(\alpha-\beta_-)-(\alpha-\beta_-)\}}{2} + \frac{\sin\{(\alpha-\beta_-)+(\alpha-\beta_-)\}}{2}\right] - \left(\frac{AB}{2}\right)^2 \left[\frac{\sin\{(\alpha-\beta_-)-(\alpha-\beta_+)\}}{2} + \frac{\sin\{(\alpha-\beta_-)+(\alpha-\beta_+)\}}{2}\right] - \left(\frac{AB}{2}\right)^2 \left[\frac{\sin\{(\alpha-\beta_+)-(\alpha-\beta_-)\}}{2} + \frac{\sin\{(\alpha-\beta_+)+(\alpha-\beta_-)\}}{2}\right] + \left(\frac{AB}{2}\right)^2 \left[\frac{\sin\{(\alpha-\beta_+)-(\alpha-\beta_+)\}}{2} + \frac{\sin\{(\alpha-\beta_+)+(\alpha-\beta_+)\}}{2}\right] \quad [4.21]$$

$$V_i \bullet V_q = \left(\frac{AB}{2}\right)^2 \left\{\left[\frac{\sin\{0\}}{2} + \frac{\sin\{2(\alpha-\beta_-)\}}{2}\right] - \left[\frac{\sin\{(\beta_+-\beta_-)\}}{2} + \frac{\sin\{(2\alpha-\beta_+-\beta_-)\}}{2}\right] - \left[\frac{\sin\{(\beta_--\beta_+)\}}{2} + \frac{\sin\{(2\alpha-\beta_+-\beta_-)\}}{2}\right] + \left[\frac{\sin\{0\}}{2} + \frac{\sin\{2(2\alpha-\beta_+)\}}{2}\right]\right\} \quad [4.22]$$

  

We will depend on the feedback filter function to remove the higher frequency terms and leave us with the transfer function of the filter and the terms remaining from the product, but we must carefully ascertain which terms will be eliminated and which will remain as shown in the following:

$$V_f = F(s)\Big|_{s\to j\varpi}\frac{A^2B^2}{8}\{\sin 2(\alpha-\beta_-) - [\sin(\beta_+-\beta_-)+\sin(2\alpha-\beta_+-\beta_-)] - [\sin(\beta_--\beta_+)+\sin(2\alpha-\beta_+-\beta_-)] + \sin 2(\alpha-\beta_+)\} \quad [4.23]$$

We note first that we can eliminate some terms because sin(x) = -sin(-x), and the term with arguments in $\beta$ alone cancel each other.

$$V_f = F(s)\Big|_{s\to j\varpi}\frac{A^2B^2}{8}\{\sin 2(\alpha-\beta_-) - \sin(2\alpha-\beta_+-\beta_-) - \sin(2\alpha-\beta_+-\beta_-) + \sin 2(\alpha-\beta_+)\} \quad [4.24]$$

$$V_f = F(s)\Big|_{s\to j\varpi}\frac{A^2B^2}{8}\{\sin 2(\alpha-\beta_-) - 2\sin(2\alpha-\beta_+-\beta_-) + \sin 2(\alpha-\beta_+)\} \quad [4.25]$$

We replace our $\alpha$ and $\beta$ parameters with the original arguments, as follows:

$$V_f = F(s)\Big|_{s\to j\varpi}\frac{A^2B^2}{8}\{\sin 2((\varpi_1 t+\theta_{err})-(\varpi_0-\varpi_{Data})t) - 2\sin(2(\varpi_1 t+\theta_{err})-(\varpi_0+\varpi_{Data})t-(\varpi_0-\varpi_{Data})t)$$

  

$$+\sin 2\left(\left(\varpi_1 t+\theta_{err}\right)-\left(\varpi_0+\varpi_{Data}\right)t\right)\Big\} \qquad [4.26]$$

We simplify the terms in equation [4.26] below:

$$V_f=F(s)\Big|_{s\to j\varpi}\frac{A^2B^2}{8}\Big\{\sin 2\left(\left(\varpi_1-\varpi_0+\varpi_{Data}\right)t+\theta_{err}\right)$$

$$-2\sin 2\left(\left(\varpi_1-\varpi_0\right)t+\theta_{err}\right)$$

$$+\sin 2\left(\left(\varpi_1-\varpi_0-\varpi_{Data}\right)t+\theta_{err}\right)\Big\} \qquad [4.27]$$

We group the terms differently to express the complementary relationship to the data frequencies as follows:

$$V_f=F(s)\Big|_{s\to j\varpi}\frac{A^2B^2}{8}\Big\{\Big[\sin 2\left(\left(\varpi_1-\varpi_0+\varpi_{Data}\right)t+\theta_{err}\right)+\sin 2\left(\left(\varpi_1-\varpi_0-\varpi_{Data}\right)t+\theta_{err}\right)\Big]$$

$$-2\sin 2\left(\left(\varpi_1-\varpi_0\right)t+\theta_{err}\right)\Big\} \qquad [4.28]$$

$$V_f=F(s)\Big|_{s\to j\varpi}\frac{A^2B^2}{4}\left\{\left[\frac{\sin\left(2\left(\left(\varpi_1-\varpi_0\right)t+\theta_{err}\right)+2\varpi_{Data}t\right)}{2}+\frac{\sin\left(2\left(\left(\varpi_1-\varpi_0\right)t+\theta_{err}\right)-2\varpi_{Data}t\right)}{2}\right]\right.$$

$$\left.-\sin 2\left(\left(\varpi_1-\varpi_0\right)t+\theta_{err}\right)\right\} \qquad [4.29]$$

$$V_f=F(s)\Big|_{s\to j\varpi}\frac{A^2B^2}{4}\Big\{\Big[\cos 2\varpi_{Data}t\bullet\sin 2\left(\left(\varpi_1-\varpi_0\right)t+\theta_{err}\right)\Big]$$

$$-\sin 2\left(\left(\varpi_1-\varpi_0\right)t+\theta_{err}\right)\Big\} \qquad [4.30]$$

The feedback action of the Costas loop will ensure that the ***VCO*** matches frequencies with the $\boldsymbol{V_{in}}$ signal, and the remaining static $\boldsymbol{\theta_{err}}$ is used to drive the ***VCO***, unless we include an integrator in F(s) to ensure that the $\boldsymbol{\theta_{err}}$ also tends to zero. In either case, the phase modulation at $\boldsymbol{\omega_{Data}}$ is the only remaining AC signal, and that is the signal we remove with ***F(s)*** filtering, as well as ***F(s)*** providing additional phase margin to the loop.

In figure 4.5 below, we show the startup of the quadrature ***VCOi*** and ***VCOq*** waveforms of the VCO, and the outputs of the two multipliers, generating the ***VMi*** and ***VMq*** waveforms.

  

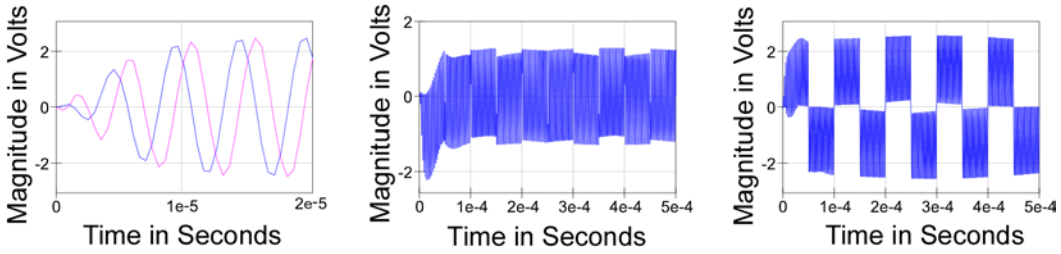


**Figure 4.5 VCOi & VCOq, VMi, and VMq Wave Forms**

The ***VCO*** is the same circuit that was used in our prior example, but in this instance we are using both of the quadrature signals. The multiplier we have employed is identical also to that used in the prior ***PLL*** example, except there are now two instances, so we have the ***VMi*** and ***VMq*** waveforms shown in figure 4.5 above.

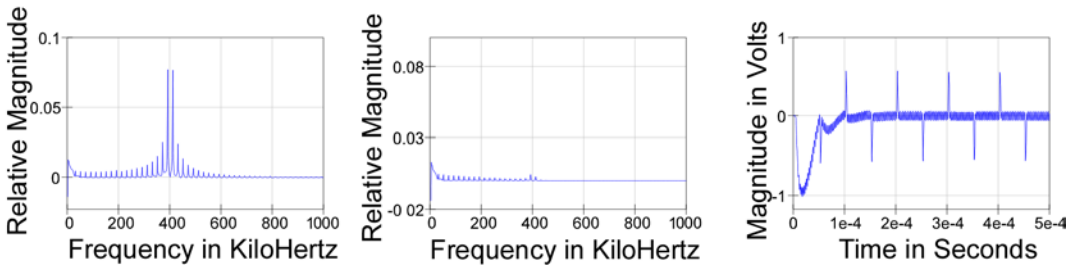


**Figure 4.6 VMi Spectrum, Vi Spectrum, and Vi Wave Form**

We apply the ***VMi*** signal to a lowpass filter to remove energy above 200 kHertz and develop the ***Vi*** signal as shown the spectra and waveform in figure 4.6 above.

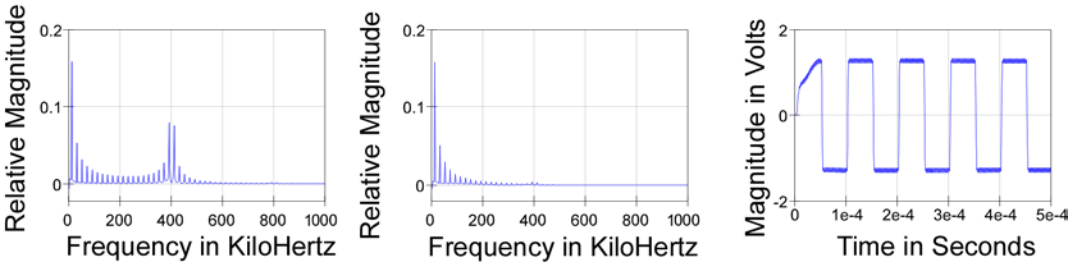


**Figure 4.7 VMq Spectrum, Vq Spectrum, and Vq Wave Form**

We apply the ***VMq*** signal to a lowpass filter to remove energy above 200 kHertz and develop the ***Vq*** signal as shown the spectra and waveform in figure 4.7 above.

  

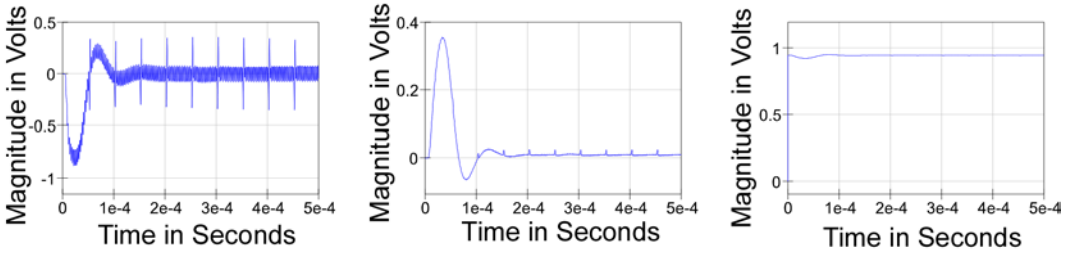


**Figure 4.8 Vph Wave Form, Vf Wave Form, and Composite VCO Control**

To complete the Costas loop, we multiply the ***Vi*** signal by the ***Vq*** signal as shown in figure 4.4 above and apply the resulting ***Vph*** product signal to a PZ compensator loop filter ***F(s)*** that is identical to the one employed in the prior ***PLL*** example to produce the ***Vf*** waveform shown. Because we have employed a duplicate of the ***VCO***, the phase detectors, and the PZ compensator loop filter, we obtain lock dynamics similar to the prior ***PLL*** example. The composite VCO control signal is also similar.

We have parameterized the lowpass filters to be identical as a 9th-order Bessel filters with a 200 kHertz characteristic frequency so that they provide no overshoot on the modulation waveform, but effectively eliminate the "sum" components of the ***VMi*** and ***VMq*** waveforms.

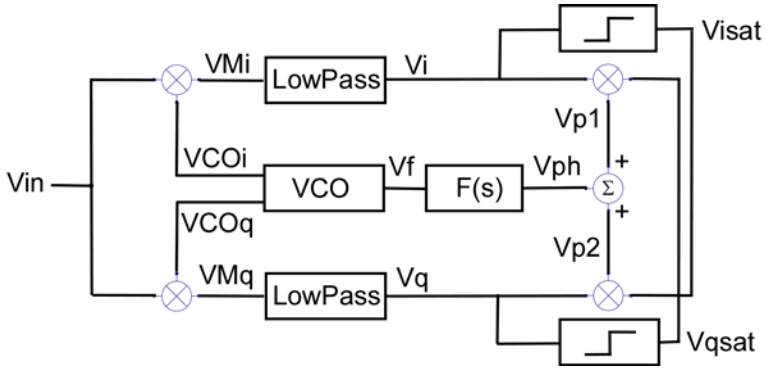


**Figure 4.9 Costas Double PLL for BPSK**

In figure 4.9 above, we show a modification to the Costas loop that includes a limiting amplifier in each filter output signal path producing the ***Visat*** and ***Vqsat*** signals from the ***Vi*** and ***Vq*** signals respectively. Much as in the original Costas loop, this "Double Loop" modification uses the product of the I and Q channel signals to produce the phase error signal ***Vph*** sent to the ***F(s)*** loop filter. In this implementation, the extra gain of the limiting amplifiers increases the effective phase detector gain, as does the summation of the two products, so the F(s) filter is modified experimentally to reduce its gain in compensation. We see the results of producing the two products in figures 4.10 and 4.11 below.

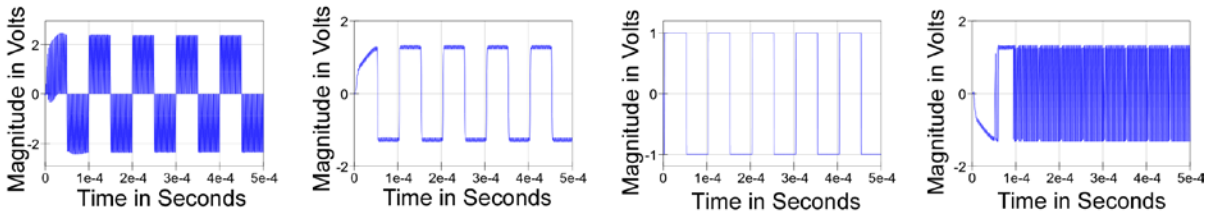


**Figure 4.10 Costas Double PLL *VMq, Vq, Vqsat,* and *Vp2***

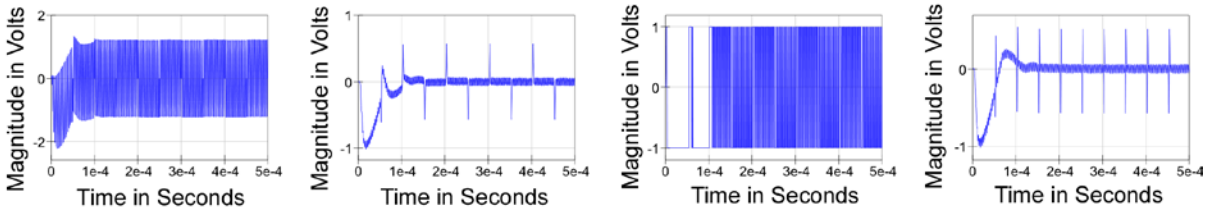


**Figure 4.11 Costas Double PLL *VMi, Vi, Visat,* and *Vp1***

In figures 4.10 and 4.11 above, we see the mixer output waveforms ***Vmi*** and ***VMq***, much the same in appearance as we saw in the original Costas loop in figure 4.5 above. Likewise, we we see the ***Vi*** and ***Vq*** waveforms much as we saw in figures 4.6 and 4.7 above. We now present the new signals ***Visat*** and ***Vqsat*** as the outputs from the hard limiting amplifiers associated with the ***I*** and ***Q*** channels. We also present two product signals, ***Vp1*** and ***Vp2*** with ***Vp1*** similar in appearance to the ***Vph*** signal of figure 4.8 in the original Costas loop. The new ***Vp2*** signal has high frequency components that are primarily the result of the limiter amplifying the remaining high frequency components of the ***I*** channel ***Visat*** signal. After the summation is performed, and the result applied to the ***F(s)*** loop filter, though, the resulting feedback signal and ***VCO*** control signals shown in figure 4.12 below are similar to the counterparts shown in figure 4.8 above.

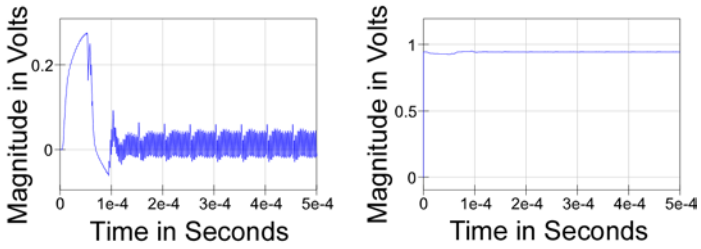


**Figure 4.12 Costas Double Vf and Composite VCO Control Signals**

  

We have shown this configuration in figure 4.9 and illustrated that equivalence to the original Costas loop because it leads us to the Costas "Double Loop" implementation shown in figure 4.13 below with the important modification of the ***Vp1*** and ***Vp2*** signals combined as a difference rather than a sum. The ***Vp1*** and ***Vp2*** signals are combined as a difference in figure 4.13 to emphasize the separation of the I and Q channel signals carrying different information as shown below.

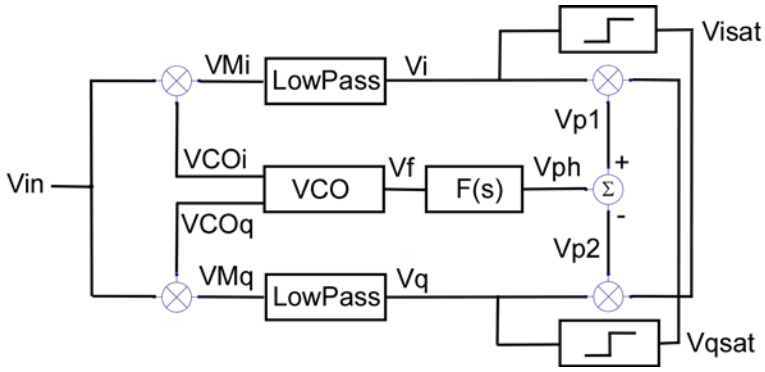


**Figure 4.13 Costas Double PLL for QAM and QPSK**

We generate a Quadra-Phase Shift Keyed signal at 200 kHertz using the data signals in figure 4.14 below with the resultant wideband spectrum. We pass the signal with that spectrum through a bandpass filter limiting the bandwidth to 50 kHertz around the 200 kHertz center frequency symmetrically. That resultant signal is used as ***Vin*** to the Costas Double Loop.

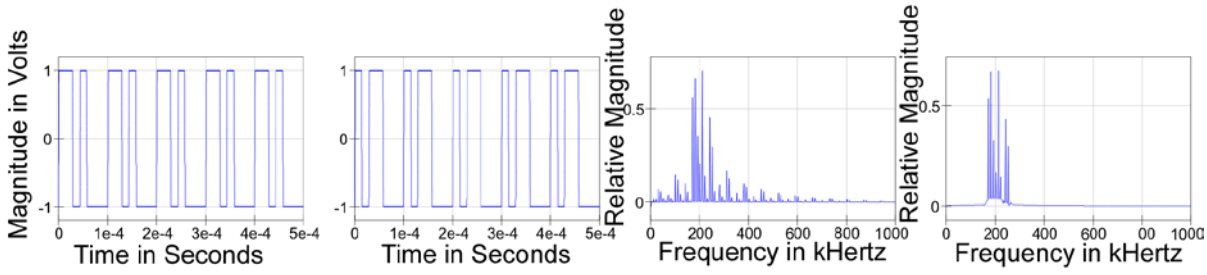


**Figure 4.14 QPSK I and Q Data, Wideband Spectrum, Bandpass Filtered Spectrum**

Much as we showed with the BiPhase example, we produce the ***Vmi***, ***VMq***, with the filtered ***Vi*** and ***Vq*** signals shown in figures 4.15 and 4.16 below and derive the ***Visat*** and ***Vqsat*** signals from the ***I*** and ***Q*** channel signals. It is the ***Vp1*** and ***Vp2*** signals that are presented to the summing amplifier that produces the phase lock control feedback signal.

  

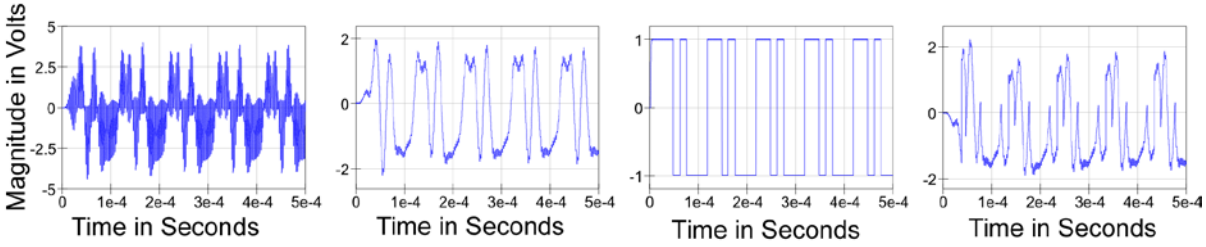


**Figure 4.15 Costas Double QPSK PLL *VMq, Vq, Vqsat,* and *Vp2***

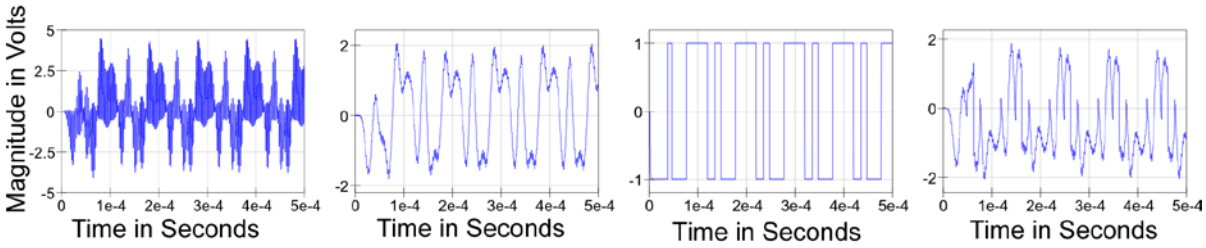


**Figure 4.16 Costas Double QPSK PLL *VMi, Vi, Visat,* and *Vp1***

The ***Vp1*** and ***Vp2*** signals shown above in figures 4.15 and 4.26 produce the difference signal shown as ***Vph*** in figure 4.17 below. The same loop filter we have used consistently for the Costas Double Loop structure is employed again to produce the Vf feedback signal with the resultant Composite VCO Control signal shown in figure 4.17 below

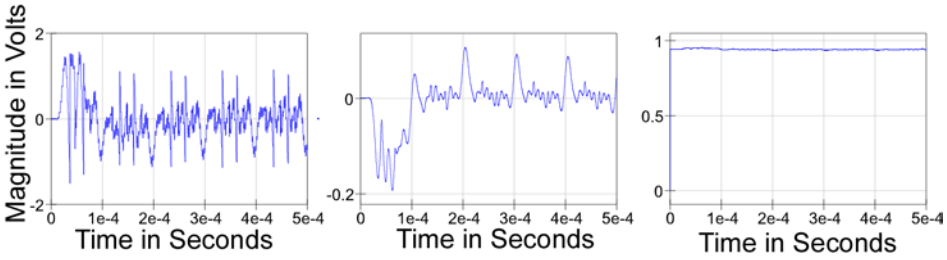


**Figure 4.17 Costas Double QPSK Vph, Vf and Composite VCO Control Signals**

We have employed the Costas Double Loop to retrieve a replica of the quadrature pair employed at 200 kHertz to produce the QPSK stimulus for the structure. In figures 4.18 and 4.19 below, we show that the ***Visat*** and ***Vqsat*** have retrieved replicas of the data with one exception.

  

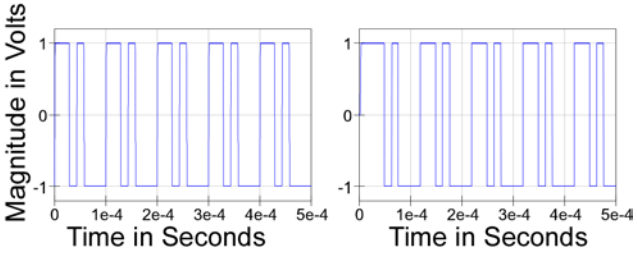


**Figure 4.18 Costas Double QPSK PLL Q Data and Vqsat**

In figure 4.18 above, we show that the data at the ***Vqsat*** signal is a replica of the ***Q*** channel data employed to modulate the QPSK signal. The replica is delayed a few microseconds as a consequence of the group delays encountered in the bandpass filter, as well as in the lowpass Bessel filter in the Q channel of the Costas loop.

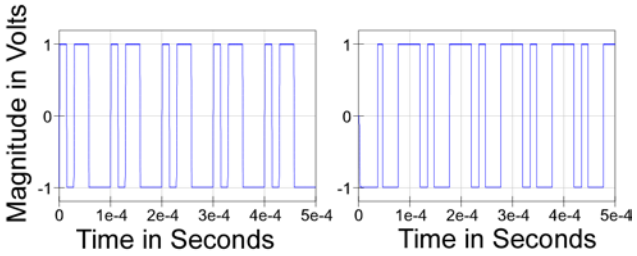


**Figure 4.19 Costas Double QPSK PLL I Data and Visat**

In figure 4.19 above, we show that the data at the ***Visat*** signal is a replica of the ***I*** channel data employed to modulate the QPSK signal. The replica is delayed a few microseconds as a consequence of the group delays encountered in the bandpass filter, as well as in the lowpass Bessel filter in the ***I*** channel of the Costas loop. Also, the data is produced in a complement form as a consequence of the uncertainty of the lock phase condition in the loop. This polarity uncertainty must be dealt with using coding in the data streams for the ***I*** and ***Q*** channels and is a well-know behavior of double-sideband, suppressed-carrier communications systems.

## 5.0 PLL Digital Frequency Synthesis for Communications

We have shown most of the PLL applications thus far in association with the reception of modulated information. In this section, we depart from purely receiving functions to more general applications associated with providing frequency sources. The function can be associated with receive, transmit, or computing and other functions. In some cases, we wish to provide a frequency reference for converting a signal either up or down the frequency

scale, or in some instance we wish to provide a frequency that avoids other uses. Although some applications employ analog, continuous-time methods, we shall discuss digital frequency synthesis in this section.

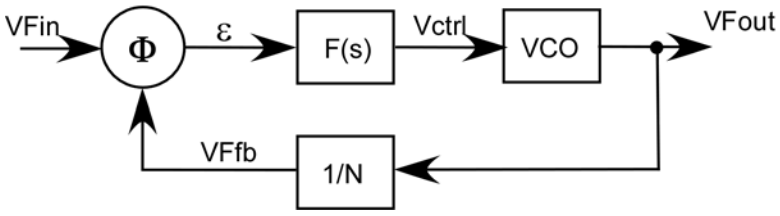


**Figure 5.0 Digital PLL System Block Diagram**

In figure 5.0 above, we have re-arranged the PLL blocks and added the ***1/N*** function block. In this system, the input signal $V_{Fin}$ is a reference frequency, and $V_{Fout}$ is the output signal and it is the relationship of the two frequencies that is important to the correct function of the system. As we develop the digital frequency synthesis topic, we will make implementation changes, but we will always utilize this fundamental architecture.

As with the analog approach, we can make assumptions about the "lock" condition and show how we ensure that the condition occurs. For the block diagram shown, a lock condition occurs when $V_{Ffb}$ is controlled to be equal to $V_{Fin}$, and any phase difference is used to produce the $\varepsilon$ error signal for feedback control of the ***VCO***.

For now, let us examine the use of the Exclusive-Or (***XOR***) logic gate as a phase detector between two digital square wave shapes. This implementation is useful as an introduction, but we will soon replace it with a more sophisticated phase detector.

**Table 5.0 XOR Truth Table**

| A | B | XOR |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

In table 5.0 above, we see that the XOR output is a logic "1" whenever the two waveforms do not match, and a logic "0" whenever they do match. We illustrate in figure 5.1 below, the ***A*** and ***B*** inputs and the ***XOR*** output, as well as the average DC value associated with the pulse-width of the ***XOR*** output.

  

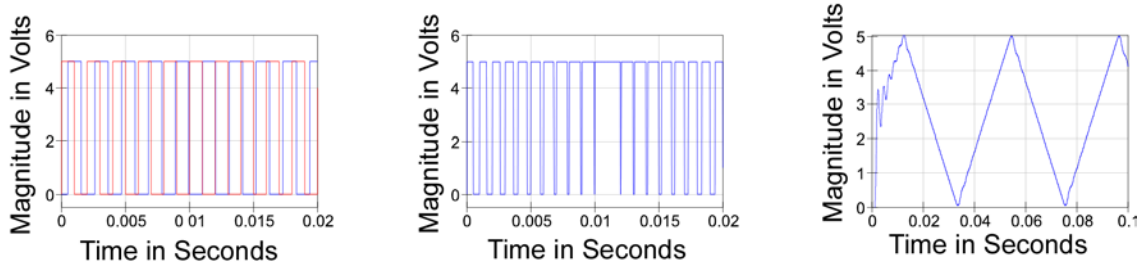


**Figure 5.1 A and B XOR Inputs, XOR Output, and Average XOR DC Voltage**

The ***A*** and ***B*** waveforms are square waves and the frequency of the ***A*** and ***B*** waveforms are different by ~10%, with ***B*** > ***A*** in frequency. The ***XOR*** provides a duty-cycle that is directly proportional to the phase difference and repeats cyclically at the difference frequency. A filter that rejects high frequency mixing harmonics provides the average DC value of the ***XOR*** output waveform. We see in figure 5.2 below the spectrum of the ***A*** and ***B*** waveforms, as well as the ***XOR*** spectrum.

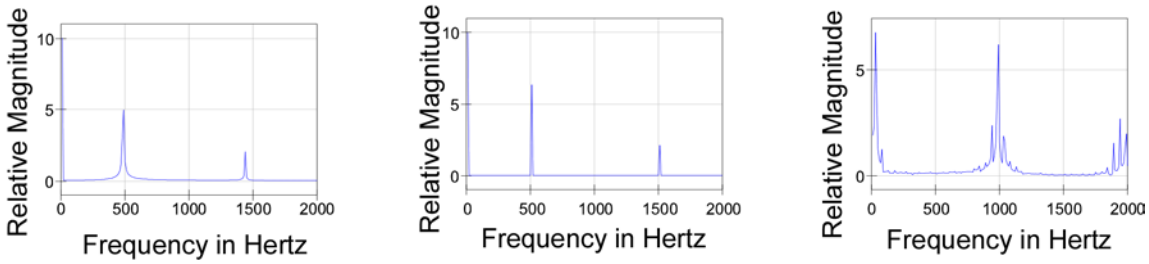


**Figure 5.2 A Spectrum, B Spectrum, and XOR Plus 2.5 VDC Offset Spectrum**

We note in figure 5.1 above, that the phase difference resulting in the difference frequency provides a triangular waveform and is “linear” over a wider phase range than the prior multiplier block used with sine wave shapes. However, we are restricted to square waveshape signals because the duty-cycle of both the ***A*** and ***B*** waveforms contribute to the average DC result. Further, only half of the phase range provides the correct feedback polarity, in a similar fashion to the analog case, to achieve and hold a lock condition. The requirement for a square wave shape imposes a sever restriction on the implementation of the 1/N counter structure because it is difficult to obtain “odd” number counts that are square waves. To address these and other concerns, we introduce the Phase-Frequency Detector (PFD) with the state-machine state map shown in figure 5.3 below.

  

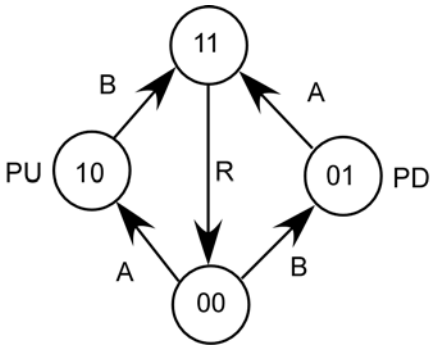


**Figure 5.3 Phase-Frequency Detector (PFD) State Map**

The Phase-Frequency Detector (***PFD***) is implemented using two edge-triggered flip-flops, each triggered from one of the frequency sources to be compared. The initial state is the "))" state, usually initialized by a start-up circuit. Whichever source occurs first triggers one of the flip-flops. We consider the ***A*** waveform to be the $V_{Fin}$ frequency reference, and the ***B*** waveform to be under control of the ***VCO*** and the feedback loop. In this context, the ***PU*** designation refers to a "Pull-Up" of the ***VCO*** frequency, and the ***PD*** designation refers to a "Pull-Down" of the ***VCO*** frequency. We have illustrated a condition with the ***B*** waveform ~10% higher than the ***A*** frequency, and will require the ***VCO*** to decrease its frequency. We have increased both ***A*** and ***B*** waveform frequencies by 10 times to near 5 kHertz for the ***PFD*** example.

We see in figure 5.4 below the implementation of the state machine. The ***B*** waveform occurs sooner than the ***A*** waveform and the state machine makes the transition from the "00" state to the "01" state and remains until the ***A*** waveform causes the transition to the "11" state. As soon as the "11" state is entered, an asynchronous "R" reset signal is generated and it resets both flip-flops. To ensure that the machine reaches the correct "00" state, the R signal is latched and removed only after the "00" state is entered.

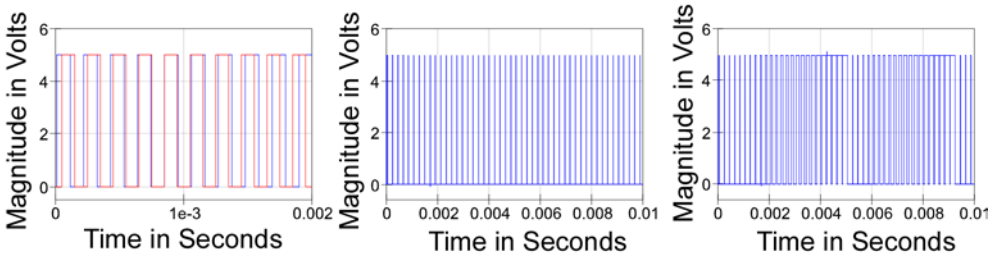


**Figure 5.4 A and B Pulses, PU Waveform, and PD Waveform**

  

In figure 5.4 above, we see that the higher frequency ***B*** waveform consistently causes the same sequence in the state machine, but with varying pulse-width results in the ***PD*** signal. We show a detail of the same waveforms in figure 5.5 below at the instant when the ***PD*** signal reaches maximum pulse width and begins a new sequence from a minimum pulse width. At the end of each ***PD*** period, the "11" state is entered and both ***PU*** and ***PD*** signals are active. We have emphasized the ***PU*** waveform so that it can be seen and discriminated at the end of the ***PD*** periods.

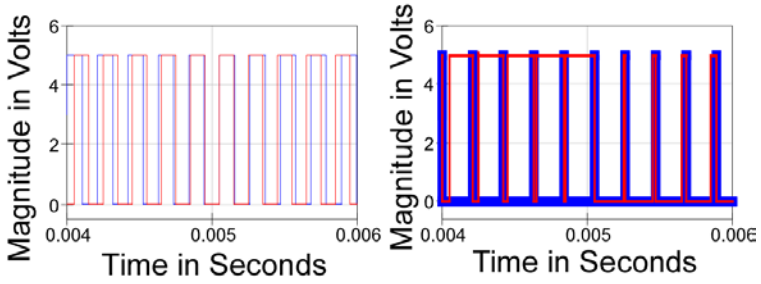


**Figure 5.5 A and B Pulses, PU and PD Waveform Details**

When the ***PFD*** state machine is in a "lock" condition, the ***PU*** and ***PD*** pulses are nearly equal because the edges that trigger the flip-flops occur nearly simultaneously. The pulses are directed to another implementation known as a "Sink-Source-Float" (***SSF***) Phase Detector, with the ***PU*** pulses introducing a charge-pump current into the ***F(s)*** loop filter that raises the ***VCO*** frequency and ***PD*** pulses introducing a charge-pump current into the ***F(s)*** loop filter that lowers the ***VCO*** frequency. The ***PU*** and ***PD*** signals cause equal, but oppositely directed currents into the ***F(s)*** loop filter, and the magnitude of the error-correction signal is proportional to the pulse-width of the signals.

When "lock is achieved, the ***PU*** and ***PD*** magnitudes of the error-correction signal are consequently near zero because the ***F(s)*** loop filter nearly always uses at least one integrator and it holds the static correction required for the lock. Only small corrections are occasionally required to correct for noise generated within the loop. Further, however, both the ***PU*** and ***PD*** pulses extend from zero pulse-width to a maximum of one cycle, or $2\pi$ radians. The implication is the entire control range is $4\pi$ radians with the nominal operating point following a $2\pi$, or 200 μsec one-cycle delay. The delay is unavoidable using the combined ***PFD*** with ***SSF*** phase detector.

  

The ***SSF***, being a bi-directional current source, is best used with the ***F(s)*** loop filter implementation consisting of the ***Z(s)*** impedance shown in figure 5.6 below.

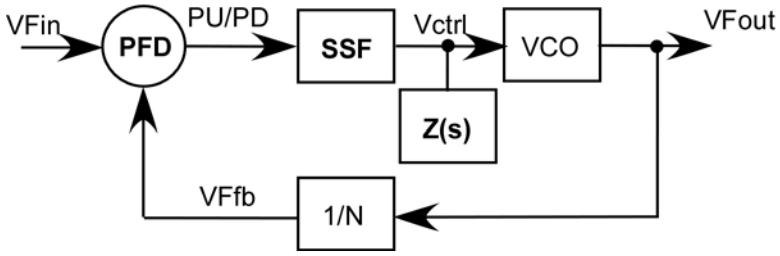


**Figure 5.6 Digital PLL System Block Diagram with PFD, SSF, and Z(s) Implementation**

We see in figure 5.6 above that the ***PFD***, ***SSF***, and ***Z(s)*** block combination has replaced the ***Φ*** phase detector and ***F(s)*** from figure 5.0, with an equivalent behavior. Insofar as the ***PFD*** combined with the ***SSF*** provides a Pulse-Width-Modulated (***PWM***) current source, we use a transfer function much like a transconductance, but parameterized in Ampere/radian to define the current delivered into the ***Z(s)*** impedance and producing the ***Vctrl*** voltage. We define the relationship for the ***PFD*** and ***SSF*** combination as:

$$\frac{I_{SSF}}{2\pi} = K_{SSF} \qquad [5.0]$$

And we combine $K_{SSF}$ with ***Z(s)*** to produce:

$$V_{ctrl} = K_{SSF} Z(s) \qquad [5.1]$$

To obtain the PZ compensation we require, we implement the ***Z(s)*** with the combination of components show in figure 5.7 as follows.

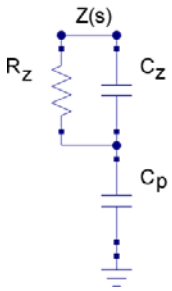


**Figure 5.7 Z(s) Implementation**

  

$$Z(s) = \frac{1}{C_p s} + \left( \frac{\frac{R_z}{C_z s}}{R_z + \frac{1}{C_z s}} \right) = \frac{1}{C_p s} + \left( \frac{R_z}{R_z C_z s + 1} \right) \quad [5.2]$$

$$Z(s) = \frac{(R_z C_z s + 1) + R_z C_p s}{C_p s (R_z C_z s + 1)} \quad [5.3]$$

$$Z(s) = \frac{1}{C_p s} \frac{(R_z (C_p + C_z) s + 1)}{(R_z C_z s + 1)} \quad [5.4]$$

And we define:

$$\tau_{Int} = \frac{C_p}{K_{SSF}} \quad [5.5]$$

$$\tau_P = R_z C_z \quad [5.6]$$

$$\tau_Z = R_z (C_p + C_z) \quad [5.6]$$

With the parameterization above, we achieve the requisite PZ compensation form that we developed in prior sections.

We continue development of the system of figure 5.6 above with a discussion of the implication of the ***1/N*** frequency divider/counter function shown in both figures 5.0 and 5.6 above. With the loop in a locked condition and the phase error maintained within a single cycle of lock range, the $V_{Fin}$ frequency reference is consequently equal to $V_{Fout}/N$. In terms of generating a range of frequencies, simplistically, we need "only" change the value of the "***N***" in the counter. Unfortunately, however, the interposed ***1/N*** has the effect of reducing the $K_{VCO}$ gain constant to a $K_{VCO}/N$ value. One approach to keeping the loop dynamics constant is the scaling of the ***SSF*** current to complement any gain reductions imposed by changing the value of the "***N***" employed. For large values of "N," it may be acceptable to make no changes if the ratio of $N_{Max}/N_{Min}$ is over a sufficiently restricted range. For example, if we wish to provide a 100 kHertz "channel" spacing over a 10 MHz range from 100 MHz to 110 MHz, we require $N_{Min}$ = 1000, and $N_{Max}$ = 1100 with only a 10% variation. Many loops can be compensated to maintain stability over such a restricted range.

  

Another consideration related to the concept of the "channel" spacing relationship to the $V_{Fin}$ frequency is the constraint imposed by the $V_{Fin}$ frequency on the loop dynamics. We have a phase error signal that updates at one edge of each cycle of the $V_{Fin}$ frequency. To achieve a narrow channel spacing, we must have a small $V_{Fin}$ frequency with a less frequent loop sampling rate. The loop dynamics consideration with narrow "channel" spacing implies a slow loop response. We will discuss this issue further in a Fractional-N Synthesis approach.

## 6.0 PFD Sampling Delay

We illustrate in figure 6.0 below the PFD detail response over a four sample interval with little phase error evident.

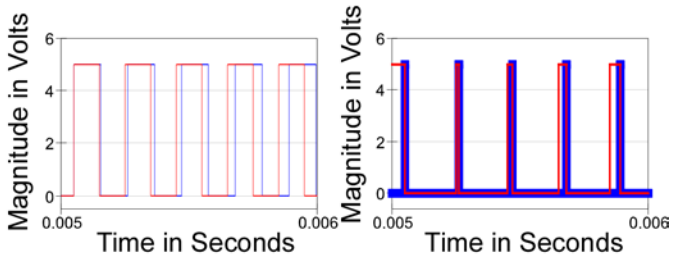


**Figure 6.0 A and B Pulses, PU and PD Waveform Details**

We have already designated the ***B*** pulses as associated with the ***VCO***, and the resulting ***PD*** waveform as the error signal. If we consider the rising edge of the ***A*** pulses, associated with the $V_{Fin}$ timing reference, we see that the ***PD*** waveform appears before the timing reference, and could extend for nearly the entire prior sampling period. Likewise, if a ***PU*** pulse were to appear, it too would commence on the rising edge of the ***A*** pulses and extend for nearly an entire sampling period. Because our system cannot predict the outcome of a PFD phase measurement, we realize that the PFD phase error signal that is a response to a previous error is a pulse near the rising edge of the next following ***A*** pulse. A full 200 μsec cycle of delay is $360^o$ at $F = 1/T_S = 5$ kHertz and $180^o$ at half that frequency, or the Nyquist rate. The delay causes a phase proportional to frequency and reaches a full $360^o$ at the sampling frequency.

The effect of sampling also generates a frequency dependent magnitude of the $\cos(2\pi f/F_s)$ resulting in a notch at half the sampling rate as illustrated in figure 6.1 below.

  

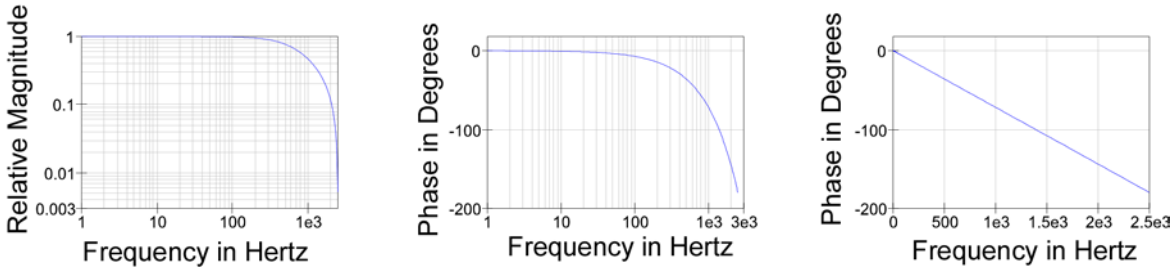


**Figure 6.1 Notch Magnitude, Phase on Logarithmic Scale, and Phase on Linear Scale**

We recall that the $V_{Fin}$ reference frequency is 5 kHertz in this example and the Nyquist frequency is 2.5 kHertz as a result. Because we cannot operate above the Nyquist rate without aliasing and loss of control, we cannot employ a unity-gain bandwidth that even approaches the Nyquist frequency and expect a stable loop.

## 7.0 PFD SSF Open and Closed Loop Stability

We illustrate in figure 7.0 below the Frequency domain Bode Plot for the combined ***VCO***, ***1/N***, ***PFD***, and ***SSF*** open-loop characteristic model.

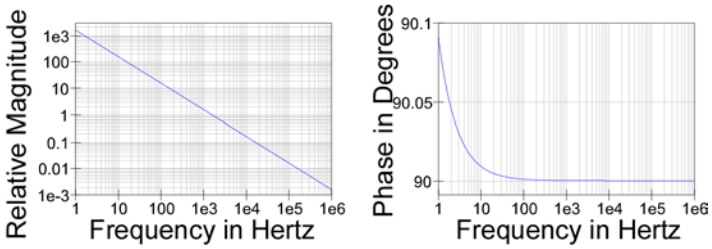


**Figure 7.0 VCO, 1/N, PFD, and SSF Open-Loop Model**

In figure 7.0 above, we show the open-loop model for the combined ***VCO***, ***1/N***, ***PFD***, and ***SSF*** components. The model in equation [7.0] below includes all components except the F(s) loop filter and the sampling delay effects shown later.

$$\frac{K_\phi}{N} K_{SSF} \phi_{VCO}(s) = \frac{K_{Oppen-Loop}}{s} \qquad [7.0]$$

The combined effects produce an integrator pole at ~1.5 kHertz, with the expected –90° phase shift associated with the integrator.

  

In similar fashion to the analog PLL Loop introduced in prior discussions, we include the PX compensator shown in figure 7.1 below and described by the combination of the SSF transconductance impinging on the ***Z(s)*** described in the prior section to produce the F(s) transfer function required.

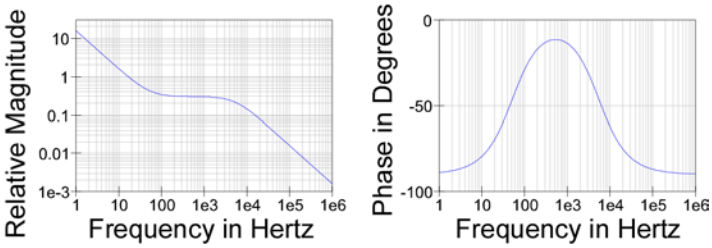


**Figure 7.1 SSF Transconductance with Z(s) to Produce F(s) PZ Compensator Model**

For this implementation with the characteristics shown in figure 7.1 above, the $K_{SSF}$ = $10^{-4}$ S, $C_p$ = 1μF, $R_z$ = 3kΩ, and $C_z$ = .01μF, so that we produce the following:

$$F_{Int} = \frac{1}{2\pi\tau_{Int}} = \frac{K_{SSF}}{2\pi C_p} = 15.9Hz \qquad [7.1]$$

$$F_p = \frac{1}{2\pi\tau_p} = \frac{1}{2\pi R_z C_z} = 5310Hz \qquad [7.2]$$

$$F_p = \frac{1}{2\pi\tau_z} = \frac{1}{2\pi R_z\left(C_p + C_z\right)} = 52.1Hz \qquad [7.3]$$

In figure 7.2 below, we include the effect of the discrete-time sampler on the PZ compensator model and show the result up to the 2.5 kHertz Nyquist notch frequency.

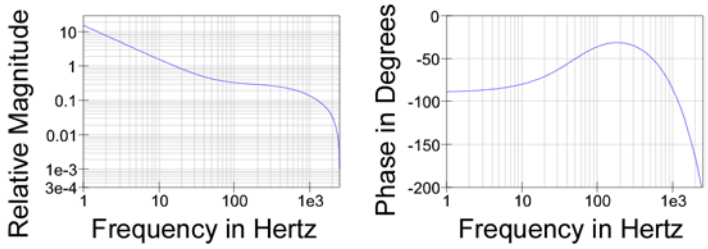


**Figure 7.2 F(s) PZ Compensator Model with Discrete-Time Sample Effects**

In figure 7.2 above, we see that the 2.5 kHertz Nyquist notch effects limit the range of compensation to below ~100 Hertz.

  

In figure 7.3 below, we illustrate the entire open-loop model, as follows:

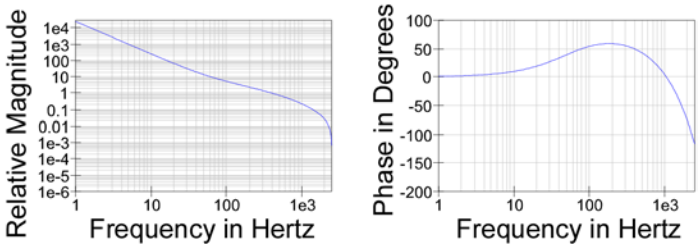


**Figure 7.3 Entire PLL Open-Loop Model with Discrete-Time Sample Effects**

In figure 7.3 above, we see that the unity-gain frequency is ~350 Hertz, and at that frequency, the phase margin is ~52 degrees. This value of phase margin is stable, but is not optimal for tracking purposes, but does support a fast acquisition as shown in the abstract closed-loop model shown in figure 7.4 below.

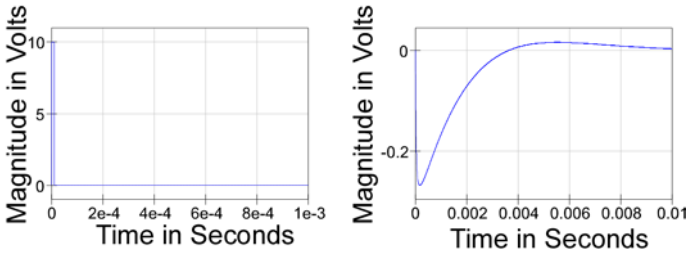


**Figure 7.4 Entire Closed Open-Loop Model Transient Pulse Response**

The abstract model tells us to expect the loop to first reach zero phase error in ~4 msec, with a small overshoot and “ringing” behavior. In figure 7.5 below, we see the PLL response:

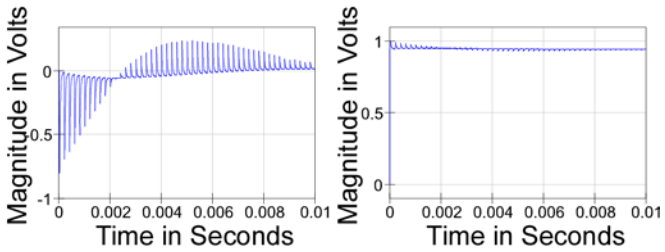


**Figure 7.5 Entire Frequency-Synthesis PLLTransient Pulse Response**

  

In figure 7.5 above, we see the actual Frequency Synthesis PLL control response. The panel on the left includes the feedback signal applied to the VCO, but the panel to the right also includes the offset voltage that places the VCO "near" the initial frequency. We will return to this result in the discussion that follows.

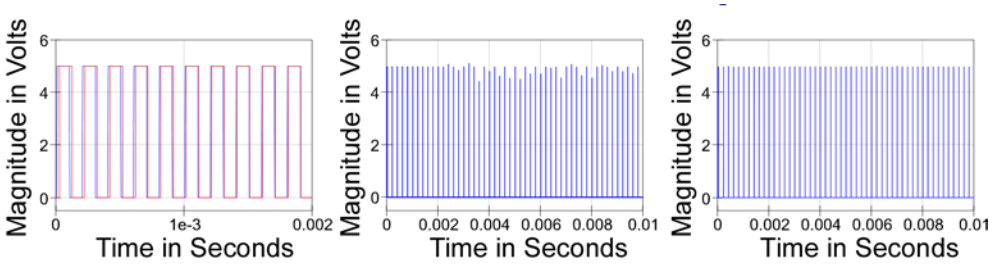


**Figure 7.6 A and B (VCO/N) Pulses, PU Waveform, and PD Waveform**

We see in figure 7.6 above that the closed loop feedback provides the control using the ***PU*** and ***PD*** pulses to minimize the phase error between the ***A*** reference frequency and the ***B*** feedback frequency.

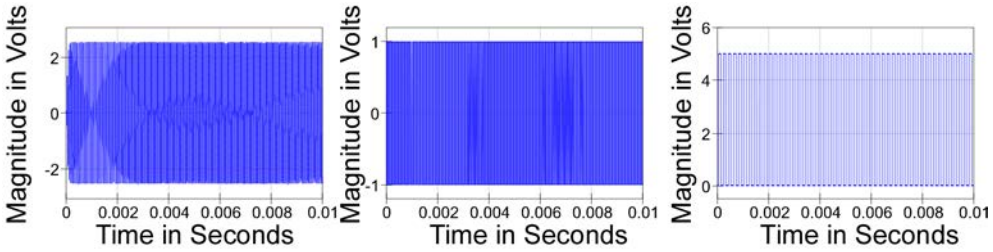


**Figure 7.7 VCO Sine Waveform, VCO Pulse Waveform, and 1/N Waveform**

In the example, N = 4 and the wave forms are shown in figure 7.7 above and figure 7.8 below.

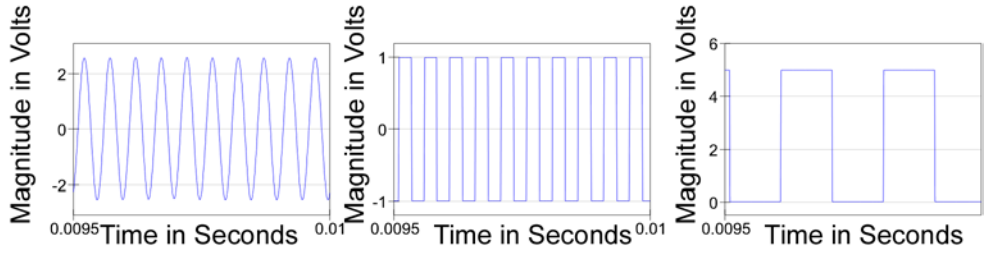


**Figure 7.8 VCO Sine Waveform, VCO Pulse Waveform, and 1/N Waveform Details**

  

It is clear in figure 7.8 above that the ***VCO*** frequency is four times the ***B*** waveform compared in the ***PFD*** with the $V_{Fin}$ ***A*** signal.

In figure 7.9 below, we show the frequency domain spectrum of the control signal in the leftmost panel of figure 7.5 that provides the feed back control to the VCO. We observed the discrete-time pulse artifacts on the average control signal and in figure 7.9 below, we see the consequences in the frequency domain.

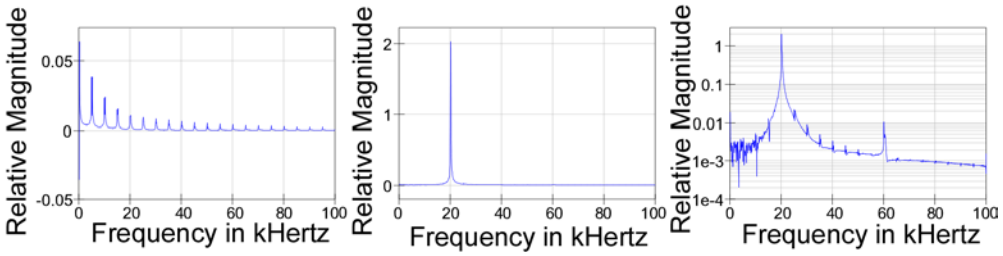


**Figure 7.9 VCO Control Spectrum, Sine Spectrum, and Sine Spectrum Details**

In figure 7.9 above, the "narrow" error pulses generated by the ***PU*** and ***PD*** phase errors occur at the 5 kHertz sampling rate and result in spectral control components at multiples of that 5 kHertz sampling rate on the ***VCO*** control signal. Because the sum of the feedback and the offset reduces the control component, on the linear magnitude scale of the center panel, not much effect is evident, however, on the logarithmic magnitude of the rightmost panel, the "spurious" signals are evident.

The effect of the spurious signals increase in proportion to the value of "N" employed. We have used N = 4 for our example, but discussed the possibility of values three orders of magnitude greater. For example, to synthesize channels with a 5 kHertz spacing at 900 MHertz, we would require values of N = ~900,000,000/5,000 or N = 36,000 for 45,000 times the spurious levels of this example. Any strategy that reduces the requirements for large values of "N" can effectively reduce the spurious artifacts on the ***VCO*** signal.

## 8.0 Fractional-N Digital Frequency Synthesis for Communications

If we were able to achieve values for the divider that were not integer values alone, we can approach the issue of "channel" spacing and loop dynamics separately. This is one objective that the Fractional-N Synthesis approach addresses.

We consider first, a change in the architecture such that we can modulate the counter modulus between values of "***N***" and "***N+1***" for periods of time. We illustrate our case using

  

the prior example of a 100 kHertz "channel" spacing over a 10 MHz range from 100 MHz to 110 MHz, but we divide the interval from "***N***" to "***N+1***" into "***M***" = 8 sub-intervals.

We employ the $V_{Fin}$ frequency reference at ***M*** x 100 KHz = 800 kHertz, allowing the loop dynamics to be ***M*** = 8X faster. To achieve the 100 kHertz channel spacing, we add a counter with its modulus ***M*** = 8 and some decoding logic to choose a fraction "***F***" of the modulus 8 count.

For ***F*** intervals, we employ the divider ***N +1*** value, but for the (M – F) remainder of the count we employ the divider ***N*** value. In this simple fashion, over M successive periods, we have used F*(N + 1) plus (M – F)*N for out feedback counter. The average count is:

$$N_{Average} = \frac{F(N+1)+(M-F)N}{M} = \frac{FN+F+MN-FN}{M} = \frac{F+MN}{M} = N+\frac{F}{M} \qquad [8.0]$$

The average divider count value equals the modulus ***N + F/M***, achieving a "fractional-***N***" value. Unfortunately, for "***F***" periods, we will have a phase error of one polarity and for the remaining "***M – F***" periods, we will have a phase error of zero or the opposite polarity and the combined periodic error signals will generate a spurious response by "Frequency Modulation" of the ***VCO***, despite the average frequency being correct.

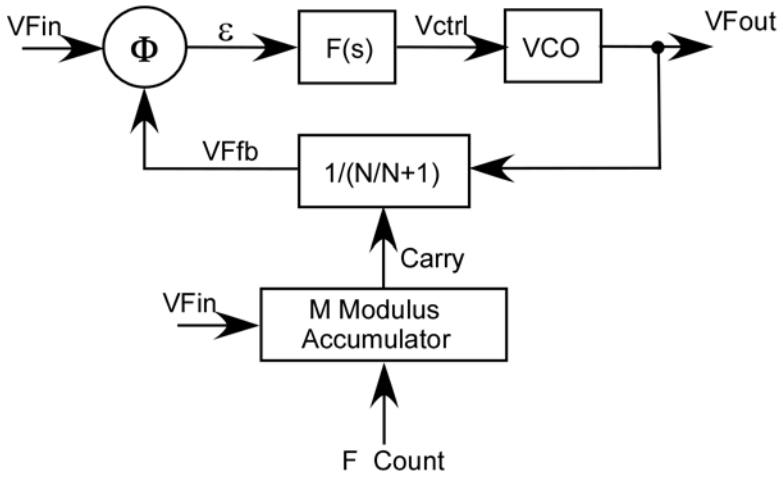


**Figure 8.0 Averaging Fractional-N Synthesizer**

  

With the averaging Fractional-N synthesis, we are faced with the issue of the phase error increments each cycle. In figure 8.1 below, we illustrate a case with the "***F***" value of seven cycles of "***N***" counts for the "***M***" value of eight periods.

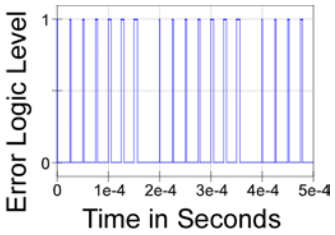


**Figure 8.1 Fractional-N Synthesis**

With the case of seven cycles of "***N***" counts and one cycle of "***N+1***" counts, we encounter incrementally increasing phase error for all but one cycle of zero error. Although we are sampling at eight times the original 5 kHertz rate, there is still a 5 kHertz repetition pattern in the phase error.

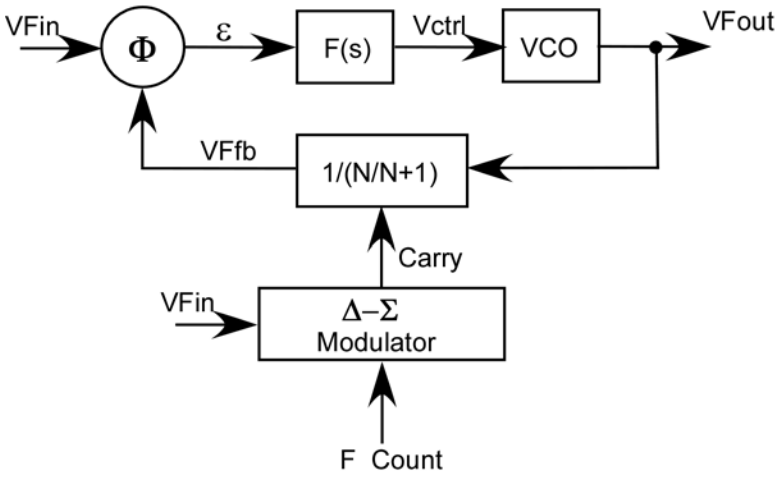


**Figure 8.2 Δ–Σ Fractional-N Synthesizer**

With the case of the ***Δ–Σ*** modulator, the "pattern" of "***N***" counts and "***N+1***" counts is modified by feedback to randomize and spread the energy to higher parts of the spectrum. Some solutions use additional counter structures to include "***N,***" "***N+,1***" and "***N+2***" or higher counters to further shape the "noise" introduced by "oversampling" in the Fractional-N arrangement. In all cases, a second-order, or usually third-order modulator, is employed to avoid cyclic "tones" from the ***Δ–Σ*** modulator itself.

  

The design of the $\Delta$–$\Sigma$ modulator is beyond the scope of this course, but is mentioned here because it provides excellent performance for reducing noise, increasing loop bandwidth, and decreasing lock times for a fractional-N frequency synthesizer.

## 9.0 Summary and Conclusions

We have introduced the Phase-Lock Loop (PLL) with considerations from classical feedback theory producing a simple analog loop for demonstration purposes.

We have analyzed the components, linearizing them as required and showed the second-order nature of the loop with the PZ compensation filter for stability.

We demonstrated the PLL capability as a Frequency-Shift Keyed (FSK) receiver demodulator for a Frequency-Modulated (FM) signal.

We introduced the Costas Loop variant of the PLL for double-sideband, suppressed-carrier synchronization using a Bi-Phase modulated signal. We introduced the "Double-Loop" variant of the Costas Loop, showing the equivalence of the saturated signal paths for the Bi-Phase modulation in a summing loop, and the requirements for a difference term for Quadri-Phase Shift Keyed (QPSK) signals. We discussed and demonstrated the $180^{o}$ phase uncertainty associated with the receiver synchronization.

We introduced the digital PLL for frequency synthesis applications, demonstrating the relationships between loop bandwidth and channel spacing. We illustrated the use of the "Exclusive-OR" logic function as a phase detector and showed the advantage of the Phase-Frequency Detector (PFD) and Sink-Source-Float (SSF) implementations.

We developed the stability requirements for the components and the design of a PZ compensator for the digital PLL, including the use of a transconductance and impedance for loop filter application.

We discussed the effects of the sampling delay on the magnitude and phase characteristics of the loop.

We demonstrated the time and frequency domain performance of a macro-model using the parameters and showed that the discrete-time performance was well predicted, but that there are noise effects from the PU/PD pulses in the PFD.

  

We introduced the Fractional-N synthesis technique and contrasted the averaging and $\Delta$–$\Sigma$ modulator approaches to the oversampling used in the Fractional-N approach.

  