Switchmode Boost Power Converter Using Current-Mode Control©

By

Raymond L. Barrett, Jr., PhD, PE
CEO, American Research and Development, LLC

1.0 Switchmode Boost Power Converter Introduction and Basic Model

This course develops models of the Boost converter with duty cycle control. Basic operation, a practical set of examples, and large/small signal models are discussed. Considerations for feedforward control to address line regulation and feedback control to address load regulation of the converter are included.

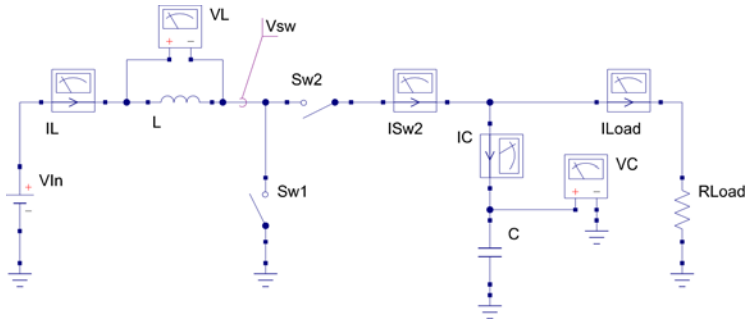

Figure 1.0 Ideal Boost Converter Schematic

We develop a constant frequency, continuous current Boost converter design, with the switching period defined below in figure 1.1 by $T_2 - T_0 = T$. The converter has two conducting states defined by periods $T_1 - T_0 = DT$ and $T_2 - T_1 = (1 - D)T$, corresponding to the two switching states. The V_{sw} node is connected using S_{w1} to ground with the duty cycle D, and a complement controlled synchronous switch S_{w2} is applied to connect the V_{sw} node to the output network during the remaining $(1 - D)$ portion of the period.

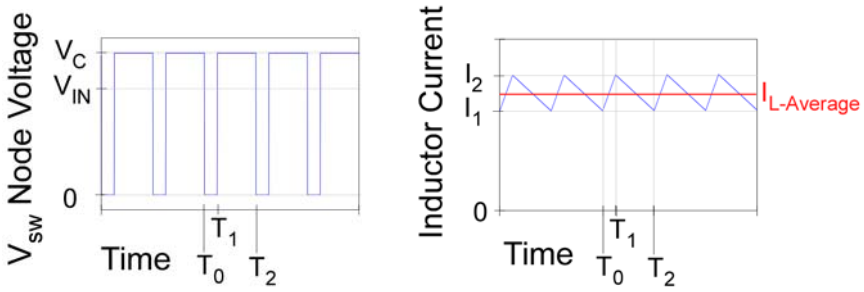

Figure 1.1 Boost Converter Inductor Operating Waveforms

The inductor cannot support a DC voltage difference across its terminals. Instead, any short-term V_L voltage difference results in a constant rate of change of current I_L through the inductor. With some V_C voltage on the capacitor, the inductor has a voltage difference V_{IN} applied during the DT interval and $V_C - V_{IN}$ applied during the $(1 - D)T$ interval.

We can equate the volt-second products and keep a zero voltage average as:

$$V_{IN}DT - (V_C - V_{IN})(1-D)T = 0 \qquad [1.0]$$

$$V_{IN}D = (V_C)(1-D) - (V_{IN})(1-D) \qquad [1.1]$$

$$V_{IN}D + V_{IN}(1-D) = V_C(1-D) \qquad [1.2]$$

$$V_C = \frac{1}{1-D}V_{IN} \qquad [1.3]$$

Equation [1.3] provides the property of the Boost converter that shows that a larger output voltage $\boldsymbol{V_C}$ can be obtained from the input $\boldsymbol{V_{IN}}$ voltage by controlling the duty cycle $\boldsymbol{D}$.

2.0 Switchmode Boost Power Converter Input/Output Current Waveforms

As shown in figure 1.1 above, the $\boldsymbol{I_{IN}}$ input current is the inductor current, and is continuous and non-zero. However, the $\boldsymbol{S_{w1}}$ current to ground during the $\boldsymbol{T_1 - T_0 = DT}$ intervals, as well as the $\boldsymbol{S_{w2}}$ current to the output voltage $\boldsymbol{V_C}$ during the $\boldsymbol{T_2 - T_1 = (1-D)T}$ intervals, as shown in figure 2.0 below, are both discontinuous.

The $\boldsymbol{I_{LOAD}}$ output current is continuous and flows through the $\boldsymbol{R_{LOAD}}$ resistor as a combination of currents from the $\boldsymbol{S_{w2}}$ current and the capacitor. Because the capacitor cannot support a continuous current, but does sink/source AC and transient currents, the average current to the load is identical to the average $\boldsymbol{S_{w2}}$ current.

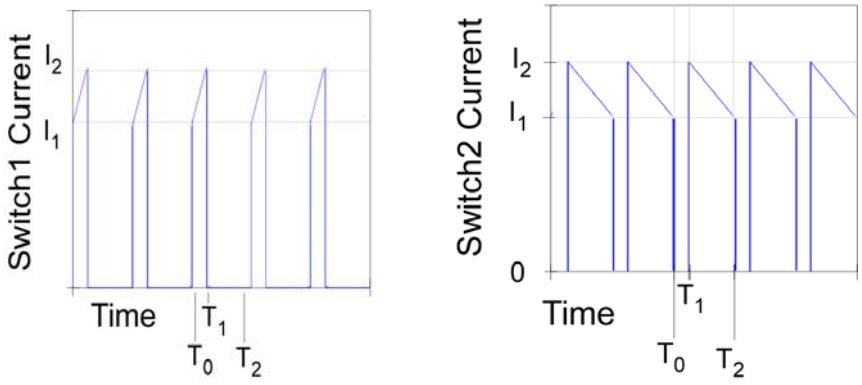

Figure 2.0 Boost Converter Switch Current Waveforms

The average input current is identical to the $I_{L\text{-}Average}$ current. The conducting S_{w2} current is the inductor current and has the same $I_{L\text{-}Average}$ current during its ON-state, but because it is non-zero only during $(1 - D)T$ intervals, its average value is $(1 - D)I_{L\text{-}Average}$ over each entire period. The average I_{LOAD} output current is also equal to the same $(1 - D)I_{L\text{-}Average}$ over each entire period.

3.0 Switchmode Boost Power Converter Input/Output Power and Efficiency

We can calculate the average input power from the product of the input V_{IN} supply times the average I_L input current as follows:

$$P_{IN} = V_{IN} \bullet I_{L-Average} \qquad [3.0]$$

Similarly, we can calculate the average output power from the product of the output V_C output times the average I_{LOAD} output current as follows:

$$P_{OUT} = V_C \bullet I_{LOAD} = V_C \bullet (1-D) I_{L-Average} \qquad [3.1]$$

If we insert equation [1.3] for the value of V_C in terms of the V_{IN} input voltage into equation [3.1], we find that the input and output average power levels are identical:

$$P_{OUT} = V_C \bullet I_{LOAD} = \frac{1}{1-D} V_{IN} \bullet (1-D) I_{L-Average} = P_{IN} \qquad [3.2]$$

The indicated 100% efficiency is not achievable because we have not accounted for losses in the switching elements, or the non-ideal practical components that we must use to implement the design, however, very high efficiencies are achievable, often exceeding 90% efficiency in a practical design.

It is the high efficiency of the switch-mode power converters that accounts for the interest, despite the complexities of the design and control means required to implement a practical design.

4.0 Output Load Current Range

The worst-case, highest current is determined by the smallest R_{LOAD} value, and in turn, the highest I_{LOAD} value. The current handling capacity of the switching devices must be sufficient to support switching the maximum I_{LOAD} value with sufficient speed to support the switching for both DT and $(1 - D)T$ periods.

The maximum value that the $\boldsymbol{R_{LOAD}}$ resistor may attain may be constrained to determine a minimum $\boldsymbol{I_{LOAD}}$ value. A minimum current value may be employed to ensure continuous load current, and to ensure stability requirements

5.0 Input/Output Ripple Current Effects in Component Value Selection

We see from equation [1.3] that the frequency does not enter directly into the relationship between the input voltage and the output voltage, but the duty cycle ***D*** is directly involved. In figure 1.1, we also see that the inductor current forms a triangular waveform between the $\boldsymbol{I_2}$ peak current, and the $\boldsymbol{I_1}$ valley current. The triangular peak-to-peak current is defined to be a "ripple current," and is an AC waveform superimposed on the average DC inductor current.

From the fundamental differential equation description of the behavior of an ideal inductor we have:

$$V_L = L \bullet \frac{dI_L}{dt} \qquad [5.0]$$

For a regime with relatively short times, relatively large inductor values, and relatively small voltages, we can approximate the relationship with line segments as follows:

$$V_L = L \bullet \frac{\Delta I_L}{\Delta t} \qquad [5.1]$$

And in more useful form:

$$\Delta I_L = I_2 - I_1 = \frac{V_L \bullet \Delta t}{L} \qquad [5.2]$$

From equation [5.2], we see that the "volt*second product" of the applied waveform can be used to determine the triangular "ripple" current between the $\boldsymbol{I_2}$ and $\boldsymbol{I_1}$ limits. To ensure continuous operation, we implement the design so that $\boldsymbol{I_1}$ remains non-zero. We select an inductor value large enough to support the "volt*second product" and satisfy the remaining design parameters.

From the fundamental differential equation description of an ideal capacitor we have:

$$I_C = C \bullet \frac{dV_C}{dt} \qquad [5.3]$$

There are two distinct time intervals for capacitor currents, the ***DT*** interval and the ***(1-D)T*** interval. During the DT interval, the capacitor is discharging into the $\boldsymbol{R_{Load}}$ load resistor alone, and the discharge follows the familiar exponential with a $\boldsymbol{CR_{Load}}$ time constant. During

the ***(1-D)T*** interval, however, there is also added the charging current through the S_{w2} switch. The waveform during each interval can obtained by solving the differential equation explicitly, but detailed waveshape information is not necessary, only the peak-to-peak voltage ripple. We use only the discharge portion of the cycle, during the ***DT*** interval to solve as follows:

$$\Delta V_C = V_C\left(1 - e^{-\frac{DT_S}{CR_{Load}}}\right) \qquad [5.4]$$

Using a "straight-line" approximation and taking the derivative of equation for the slope of the discharge line, we have:

$$\Delta V_C \cong -\frac{DT_S}{CR_{Load}}V_C \qquad [5.5]$$

Equation [5.4] offers a value for the peak-to-peak ripple voltage that can be expected to be caused by the choice of capacitor value and time interval, but it is probably more useful expressed as the ratio:

$$\frac{\Delta V_C}{V_C} \cong -\frac{DT_S}{CR_{Load}} \qquad [5.5]$$

Additional non-ideal parasitic components are needed to describe the power lost in the inductor and capacitor.

6.0 Input/Output Voltage Range Considerations

Practical applications require that we produce a controlled value for V_C over a range of input voltage V_{IN} values.

For instance, automotive applications may require a nominal 12V V_{IN} operation, but be expected to function nominally under a low battery condition below 10V, and also operate with transient V_{IN} values in excess of 52V for a few milliseconds in the case of "load-dump" of highly inductive DC motor and solenoid devices connected to that same battery/alternator system. The V_{IN} range can be >5:1 for some automotive applications.

Similarly, "line-powered" applications may be expected to function correctly with common switching circuitry when powered from 110/220V mains sources. The line-powered ranges may be ~85V from the low-line 110V source, but also as higher than 365V under high-line 220V sourcing. The V_{IN} range can be >4.5:1 for some "line-powered" applications.

Although many applications require a fixed output voltage, there are also applications that require a user-programmed output voltage also, often over a considerable range of values.

The capacitor must withstand the highest expected output voltage under both nominal and transient conditions.

The ratio of the smallest output voltage to the highest input voltage determines the smallest nominal value of duty-cycle required. Likewise, the ratio of the highest output voltage to the lowest input voltage determines the largest value of duty-cycle required.

7.0 Switchmode Boost Power Converter Line/Load Regulation Introduction

Practical applications typically require that we provide a controlled value for $\boldsymbol{V_C}$ despite changes in the input voltage $\boldsymbol{V_{IN}}$. The term "line regulation" is used to describe the resulting effect of that control effort.

Also, practical applications require that we provide a controlled value for $\boldsymbol{V_C}$ despite changes in the load current $\boldsymbol{I_{LOAD}}$. The term "load regulation" is used to describe the resulting effect of that control effort.

Practical applications use a combined strategy for controlling the duty cycle dependent on both the $\boldsymbol{V_{IN}}$ and the $\boldsymbol{V_C}$ values. That part of the control that uses the $\boldsymbol{V_{IN}}$ value to control the duty cycle is called a "feedforward" control mechanism. That part of the controller that uses the $\boldsymbol{V_C}$ value to control the duty cycle is called a "feedback" control mechanism. With current-mode control, the switching waveform depends on the inductor current waveform when the current is increasing from the connection between $\boldsymbol{V_{IN}}$ and ground. The dependency of the waveforms makes current-mode control inherently employ feedforward control.

To facilitate each form of control, a detailed small-signal model is developed so that the stability and performance of the control can be determined. However, the feedforward control lessens the changes in $\boldsymbol{V_C}$ that the feedback must deal with, making the feedback design less demanding. It is feedback control that requires a small-signal model to determine gain and phase margins, as well as any compensation required to stabilize the closed loop behavior.

8.0 Switchmode Boost Power Converter Preliminary Duty-Cycle Control Model

The Boost converter model is described using two state variables: the inductor current $\boldsymbol{I_L}$ and the capacitor voltage $\boldsymbol{V_C}$**.** The input voltage $\boldsymbol{V_{IN}}$ and the load resistance $\boldsymbol{R_{LOAD}}$ are retained to express the input and output dependencies for line and load regulation.

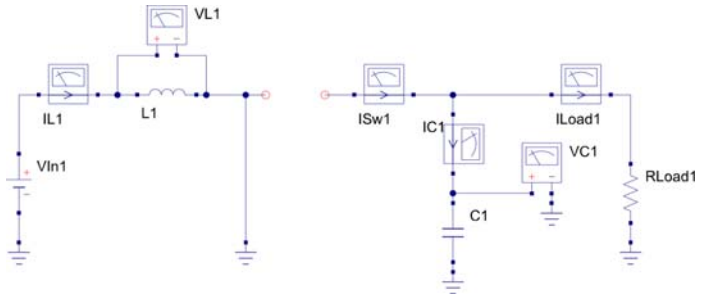

Figure 8.0 Boost Converter Schematic During the *DT* Period

Modeling begins with the topology defined in figure 8.0 during the ***DT*** interval with the grounding switch S_{w1} conducting and S_{w2} OFF. We use Kirchoff's Voltage Law (***KVL***) around the loop including V_{IN}, and ***L***, and Kirchoff's Current Law (***KCL***) at the node defined by the V_C voltage, to write two defining equations:

$$V_{IN} = V_L \qquad [8.0]$$

$$0 = I_{LOAD} + I_C \qquad [8.1]$$

Because V_L, I_{LOAD}, and I_C are not the chosen state variables, we rewrite the equations in terms of the state variables, and use the Laplace "***s***" operator to obtain the equations:

$$V_{IN} = LsI_L \qquad [8.2]$$

and

$$0 = \frac{V_C}{R_{LOAD}} + CsV_C \qquad [8.3]$$

We rewrite equations [8.2] and [8.3] into differential equation form, as follows:

$$sI_L = \frac{1}{L}V_{IN} \qquad [8.4]$$

$$sV_C = -\frac{1}{CR_{LOAD}}V_C \qquad [8.5]$$

We define a state vector composed of the two state variables:

$$X = \begin{vmatrix} I_L \\ V_C \end{vmatrix} \qquad [8.6]$$

We then express the two equations in matrix form using the state vector and build the state matrix as the expression of the two simultaneous equations. It is a matrix differential equation with the derivative of the state vector ***Xs***, expressed in terms of the state vector ***X*** itself and the $\boldsymbol{V_{IN}}$ input voltage:

$$Xs = \begin{vmatrix} 0 & 0 \\ 0 & -1/CR_{LOAD} \end{vmatrix} X + \begin{vmatrix} 1/L \\ 0 \end{vmatrix} V_{IN} \qquad [8.7]$$

The matrix differential equation [8.7] describes the behavior of the Boost converter during the time ***DT*** that the input supply is connected through the closed $\boldsymbol{S_{w1}}$ switch.

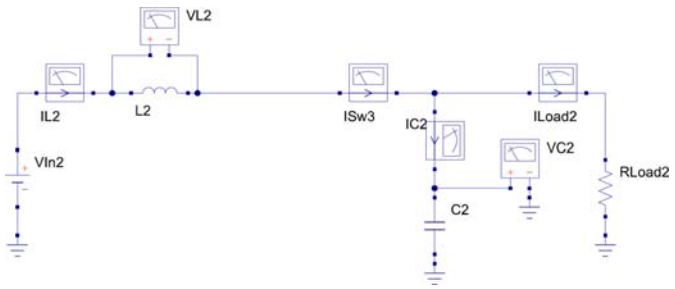

Figure 8.1 Boost Converter Schematic During the (1-*D*)*T* Period

We continue modeling with the topology defined in figure 8.1, with conduction through the synchronous switch during the ***(1-D)T*** interval, again using ***KVL*** and ***KCL*** to write two modified defining equations:

$$V_{IN} = V_L + V_C \qquad [8.8]$$

$$I_L = I_{LOAD} + I_C \qquad [8.9]$$

As before, we rewrite the defining equations:

$$V_{IN} = LsI_L + V_C \qquad [8.10]$$

$$I_L = \frac{V_C}{R_{LOAD}} + CsV_C \qquad [8.11]$$

We write equations [8.10] & [8.11] into explicit differential equation form, as follows:

$$sI_L = -\frac{1}{L}V_C + \frac{1}{L}V_{IN} \qquad [8.12]$$

$$sV_C = \frac{1}{C}I_L - \frac{1}{CR_{LOAD}}V_C \qquad [8.13]$$

Using the state vector as previously defined, we express the new matrix differential equation as follows:

$$Xs = \begin{vmatrix} 0 & -1/L \\ 1/C & -1/CR_{LOAD} \end{vmatrix} X + \begin{vmatrix} 1/L \\ 0 \end{vmatrix} V_{IN} \qquad [8.14]$$

9.0 Switchmode Buck Power Converter State-Space Average Model

Following the practice of state-space averaging, we sum ***D*** times the component matrix in equation [8.7] plus ***(1-D)*** times the component matrix in equation [8.14] to provide the state-space averaged equations:

$$Xs = D\begin{vmatrix} 0 & 0 \\ 0 & -1/CR_{LOAD} \end{vmatrix} X + D\begin{vmatrix} 1/L \\ 0 \end{vmatrix} V_{IN} + (1-D)\begin{vmatrix} 0 & -1/L \\ 1/C & -1/CR_{LOAD} \end{vmatrix} X + (1-D)\begin{vmatrix} 1/L \\ 0 \end{vmatrix} V_{IN} \qquad [9.0]$$

In equation [9.0] terms with the factor ***D*** arise from the first interval of the switching period, and terms with the ***(1-D)*** factor from the second interval of the switching period. The state-variable ***X*** is now the average for the entire switching period. We distribute algebraically the duty-cycle ***D*** dependence as follows:

$$Xs = D\begin{vmatrix} 0 & 0 \\ 0 & -1/CR_{LOAD} \end{vmatrix} X + D\begin{vmatrix} 1/L \\ 0 \end{vmatrix} V_{IN} + \begin{vmatrix} 0 & -1/L \\ 1/C & -1/CR_{LOAD} \end{vmatrix} X - D\begin{vmatrix} 0 & -1/L \\ 1/C & -1/CR_{LOAD} \end{vmatrix} X + \begin{vmatrix} 1/L \\ 0 \end{vmatrix} V_{IN} - D\begin{vmatrix} 1/L \\ 0 \end{vmatrix} V_{IN} \qquad [9.1]$$

$$Xs = D\begin{vmatrix} 0 & 0 \\ 0 & -1/CR_{LOAD} \end{vmatrix} X - D\begin{vmatrix} 0 & -1/L \\ 1/C & -1/CR_{LOAD} \end{vmatrix} X + \begin{vmatrix} 0 & -1/L \\ 1/C & -1/CR_{LOAD} \end{vmatrix} X + \begin{vmatrix} 1/L \\ 0 \end{vmatrix} V_{IN} \quad [9.2]$$

$$Xs = \begin{vmatrix} 0 & -1/L \\ 1/C & -1/CR_{LOAD} \end{vmatrix} X - D\begin{vmatrix} 0 & -1/L \\ 1/C & 0 \end{vmatrix} X + \begin{vmatrix} 1/L \\ 0 \end{vmatrix} V_{IN} \quad [9.3]$$

10.0 Boost Converter Initial Inductor Choice

We choose as a design requirement; a Boost Converter based on a nominal 10.2V to 14.7V $\boldsymbol{V_{IN}}$ range to supply 28V at $\boldsymbol{V_C}$ with 50 milli-Volt maximum ripple voltage. The converter must support a nominal 1 Ampere load. We constrain the minimum load to be 1% of the maximum value, or 10 milli-Amperes, using an internal load resistance. A 2.5 MHz switching frequency is used for the example.

We choose a 200 milli-Ampere peak-to-peak inductor current ripple as an upper limit for a nominal value.

From the $\boldsymbol{V_{IN}}$ range and the fixed 28V $\boldsymbol{V_C}$ value, we determine that the range of duty-cycle $\boldsymbol{D}$ must be 0.47 to 0.64. At 2.5 MHz, the times are 190 nsec to 254 nsec.

We use the 14.7V $\boldsymbol{V_{IN}}$ value during the shortest 190 nsec interval to determine the minimum inductor value that will support that voltage with the requisite current change, as follows:

$$0.2 = \Delta I_L = \frac{V_L}{L}\Delta t = \frac{14.7}{L}190 \bullet 10^{-9} \quad [10.0]$$

$$L = \frac{14.7}{0.2} \bullet 1.9 \bullet 10^{-7} = 13.9\mu H \quad [10.1]$$

To further address the selection of the inductor, we must consider that the Boost converter delivers a maximum of 1A at 28V or 28Watts and should not dissipate appreciable power in the inductor, while delivering that current.

The inductor must be capable of handling $\boldsymbol{I_{L\text{-}Average}}$ without saturation of the inductance, as well as have a low DC resistance. From equation [3.1], we know that $\boldsymbol{I_{Load}}$ was derived from $\boldsymbol{(1\text{-}D)\ I_{L\text{-}Average}}$ so consequently we find the maximum average inductor current as:

$$I_{L-Average} = \frac{I_{LOAD}}{1-D} = \frac{1}{1-.64} = 2.8A \qquad [10.2]$$

The power loss in the DC resistance (DCR) of the inductor is:

$$P = I^2 DCR = (2.8)^2 DCR \qquad [10.3]$$

We find a 22µH Murata component (Digikey # 811-1341-ND) that has 11mΩ □□DCR and will cause less than 1% loss at 2.8 Ampere inductor current. We consider that as acceptable.

Other considerations, including price, shielding, assembly requirements, etc., can alter other component parameters, but the inductance and DCR requirements must be met by whatever selection is made

11.0 The Simple Boost Converter Initial Capacitor Choice

We determine the minimum capacitor value from equation [5.5] as follows:

$$C_{Min} = \frac{V_C}{\Delta V_C}\frac{DT_S}{R_{Load}} = \frac{28V}{.05V} \bullet \frac{0.190 \bullet 10^{-6}\ \text{sec}}{28\Omega} = 4\mu F \qquad [11.0]$$

We can meet the capacitor requirements with a 50V 10 µF AVX multi-layer ceramic capacitor (Digikey # 478-5048-1-ND). Again, other device parameters must be considered and these selections are for illustration only.

12.0 Switchmode Boost Power Converter Small-Signal State-Space Average Model

To model the small-signal behaviors, we introduce a notation that represents a DC operating point with "capital" letters, and small signal perturbations with the smaller letters for each variable and substitute in the model we developed in equation [9.3], as follows:

$$(X+x)s = \begin{vmatrix} 0 & -1/L \\ 1/C & -1/CR_{LOAD} \end{vmatrix}(X+x)$$
$$-(D+d)\begin{vmatrix} 0 & -1/L \\ 1/C & 0 \end{vmatrix}(X+x) + \begin{vmatrix} 1/L \\ 0 \end{vmatrix}(V_{IN}+v_{IN}) \qquad [12.0]$$

We expand the terms, of equation [12.0], and remove any products of small terms as "second-order" and small enough to ignore, as follows:

$$Xs + xs = \begin{vmatrix} 0 & -1/L \\ 1/C & -1/CR_{LOAD} \end{vmatrix} X + \begin{vmatrix} 0 & -1/L \\ 1/C & -1/CR_{LOAD} \end{vmatrix} x$$
$$- D\begin{vmatrix} 0 & -1/L \\ 1/C & 0 \end{vmatrix} X - d\begin{vmatrix} 0 & -1/L \\ 1/C & 0 \end{vmatrix} X - D\begin{vmatrix} 0 & -1/L \\ 1/C & 0 \end{vmatrix} x$$
$$+ \begin{vmatrix} 1/L \\ 0 \end{vmatrix} V_{IN} + \begin{vmatrix} 1/L \\ 0 \end{vmatrix} v_{IN} \qquad [12.1]$$

From equation [12.1], we subtract the large-signal operating-point equation given in equation [9.3], as follows:

$$xs = (Xs + xs) - Xs = \begin{vmatrix} 0 & -1/L \\ 1/C & -1/CR_{LOAD} \end{vmatrix} X + \begin{vmatrix} 0 & -1/L \\ 1/C & -1/CR_{LOAD} \end{vmatrix} x$$
$$- \begin{vmatrix} 0 & -1/L \\ 1/C & -1/CR_{LOAD} \end{vmatrix} X$$
$$- D\begin{vmatrix} 0 & -1/L \\ 1/C & 0 \end{vmatrix} X - d\begin{vmatrix} 0 & -1/L \\ 1/C & 0 \end{vmatrix} X - D\begin{vmatrix} 0 & -1/L \\ 1/C & 0 \end{vmatrix} x$$
$$+ D\begin{vmatrix} 0 & -1/L \\ 1/C & 0 \end{vmatrix} X$$
$$+ \begin{vmatrix} 1/L \\ 0 \end{vmatrix} V_{IN} + \begin{vmatrix} 1/L \\ 0 \end{vmatrix} v_{IN} - \begin{vmatrix} 1/L \\ 0 \end{vmatrix} V_{IN} \qquad [12.2]$$

Collecting terms, we have the small-signal model as follows:

$$xs = \left\{ \begin{vmatrix} 0 & -\left(\frac{1}{L}\right) \\ \left(\frac{1}{C}\right) & -\left(\frac{1}{CR_{LOAD}}\right) \end{vmatrix} - D\begin{vmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & 0 \end{vmatrix} \right\} x - d\begin{vmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & 0 \end{vmatrix} X + \begin{vmatrix} \frac{1}{L} \\ 0 \end{vmatrix} v_{IN} \qquad [12.3]$$

The state-space averaged small-signal model is truly only valid for small signals. Likewise, it is only valid for small-signal perturbations with much lower frequency than the switching frequency. Serious aliasing effects can make the model unusable for frequencies approaching a large fraction of the Nyquist frequency (half the switching frequency). However, for analysis at lower frequencies to about 10% of the switching frequency, the state-space averaged model gives good results.

13.0 Boost Power Converter Small-Signal Current-Mode Control

For current programming we develop a change of control variables from the explicit duty cycle to a controlling current signal. The constraint equation is taken from the inductor current given in the first row of equation [12.3] as:

$$si_L = -(1-D)\,{}^{1}\!/_{L}\, v_c + d\,{}^{1}\!/_{L}\, V_C + {}^{1}\!/_{L}\, v_{IN} \qquad [13.0]$$

We solve for d:

$$d\,{}^{1}\!/_{L}\, V_C = si_L + (1-D)\,{}^{1}\!/_{L}\, v_c - {}^{1}\!/_{L}\, v_{IN} \qquad [13.1]$$

$$d = \frac{1}{V_C}\left[Lsi_L + (1-D)v_c - v_{IN}\right] \qquad [13.2]$$

We substitute ***d*** back into the small-signal state space model of equation [12.3], but we perform the substitution explicitly in each row, starting with the first row, as follows:

$$si_L = -(1-D)\,{}^{1}\!/_{L}\, v_c + \frac{1}{V_C}\left[Lsi_L + (1-D)v_c - v_{IN}\right]{}^{1}\!/_{L}\, V_C + {}^{1}\!/_{L}\, v_{IN} \qquad [13.3]$$

$$si_L = -(1-D)\,{}^{1}\!/_{L}\, v_c + si_L + (1-D)\,{}^{1}\!/_{L}\, v_c - {}^{1}\!/_{L}\, v_{IN} + {}^{1}\!/_{L}\, v_{IN} \qquad [13.4]$$

$$si_L = si_L \qquad [13.5]$$

Equation [14.5] shows a "tautology" by proving that the equation [13.2] for ***d*** that we obtained from the first row reduces the equation to a "simple truth." The value is a proof that we indeed have an accurate relation for ***d*** that we can use in the second row.

And from the second row of equation [12.3], we have:

$$Csv_C = (1-D)i_L - \left(\frac{1}{R_{LOAD}}\right)v_C - dI_L \qquad [13.6]$$

So, with a substitution for ***d***, we have:

$$Csv_C = (1-D)i_L - \left(\frac{1}{R_{LOAD}}\right)v_C - \frac{I_L}{V_C}\left[Lsi_L + (1-D)v_c - v_{IN}\right] \qquad [13.7]$$

$$Csv_C = (1-D)i_L - \left(\frac{1}{R_{LOAD}}\right)v_C - \left[\frac{I_L}{V_C}Lsi_L + (1-D)\frac{I_L}{V_C}v_c - \frac{I_L}{V_C}v_{IN}\right] \qquad [13.8]$$

$$Csv_C = (1-D)i_L - \left(\frac{1}{R_{LOAD}}\right)v_C - \frac{I_L}{V_C}Lsi_L - (1-D)\frac{I_L}{V_C}v_c + \frac{I_L}{V_C}v_{IN} \qquad [13.9]$$

$$Csv_C + \left(\frac{1}{R_{LOAD}}\right)v_C + (1-D)\frac{I_L}{V_C}v_c = (1-D)i_L - \frac{I_L}{V_C}Lsi_L + \frac{I_L}{V_C}v_{IN} \qquad [13.10]$$

We collect terms as follows:

$$\left[Cs + \frac{1}{R_{LOAD}} + (1-D)\frac{I_L}{V_C}\right]v_C = -\left[\frac{I_L}{V_C}Ls - (1-D)\right]i_L + \frac{I_L}{V_C}v_{IN} \qquad [13.11]$$

At the end of section 2.0, we observed that the "average $\boldsymbol{I_{LOAD}}$ output current is also equal to the same $\boldsymbol{(1-D)I_{L\text{-}Average}}$ over each entire period," and we can use the relationship to simplify equation [13.9] as follows:

$$(1-D)I_L = I_{LOAD} \qquad [13.12]$$

$$\left[Cs + \frac{1}{R_{LOAD}} + \frac{I_{LOAD}}{V_C}\right]v_C = -\left[\frac{I_L}{V_C}Ls - (1-D)\right]i_L + \frac{I_L}{V_C}v_{IN} \qquad [13.13]$$

$$\left[Cs + \frac{1}{R_{LOAD}} + \frac{I_{LOAD}}{V_C}\right]v_C = (1-D)i_L - \frac{I_L}{V_C}Lsi_L + \frac{I_L}{V_C}v_{IN} \qquad [13.14]$$

$$V_C = I_{LOAD}R_{LOAD} \qquad [13.15]$$

$$\left[Cs+\frac{1}{R_{LOAD}}+\frac{1}{R_{LOAD}}\right]v_C=(1-D)i_L-\frac{I_L}{V_C}Lsi_L+\frac{I_L}{V_C}v_{IN} \quad [13.16]$$

$$\left[Cs+\frac{2}{R_{LOAD}}\right]v_C=(1-D)i_L-\frac{I_L}{V_C}Lsi_L+\frac{I_L}{V_C}v_{IN} \quad [13.17]$$

$$\frac{2}{R_{LOAD}}\left[\frac{R_{LOAD}C}{2}s+1\right]v_C=-\left[\frac{I_L}{V_C}Ls-(1-D)\right]i_L+\frac{I_L}{V_C}v_{IN} \quad [13.18]$$

$$V_C=(1-D)I_LR_{LOAD} \quad [13.19]$$

$$\frac{2}{R_{LOAD}}\left[\frac{R_{LOAD}C}{2}s+1\right]v_C=-\left[\frac{I_L}{(1-D)I_LR_{LOAD}}Ls-(1-D)\right]i_L+\frac{I_L}{(1-D)I_LR_{LOAD}}v_{IN} \quad [13.20]$$

$$\frac{2}{R_{LOAD}}\left[\frac{R_{LOAD}C}{2}s+1\right]v_C=-\left[\frac{1}{(1-D)}\frac{L}{R_{LOAD}}s-(1-D)\right]i_L+\frac{1}{(1-D)}\frac{1}{R_{LOAD}}v_{IN} \quad [13.21]$$

$$v_C=-\frac{\left[\frac{1}{(1-D)}\frac{L}{R_{LOAD}}s-(1-D)\right]}{\frac{2}{R_{LOAD}}\left[\frac{R_{LOAD}C}{2}s+1\right]}i_L+\frac{\frac{1}{(1-D)}\frac{1}{R_{LOAD}}}{\frac{2}{R_{LOAD}}\left[\frac{R_{LOAD}C}{2}s+1\right]}v_{IN} \quad [13.22]$$

$$v_C=-\frac{(1-D)}{2}R_{LOAD}\frac{\left[\frac{1}{(1-D)^2}\frac{L}{R_{LOAD}}s-1\right]}{\left[\frac{R_{LOAD}C}{2}s+1\right]}i_L+\frac{1}{2(1-D)}\frac{1}{\left[\frac{R_{LOAD}C}{2}s+1\right]}v_{IN} \quad [13.23]$$

Armed with equation [13.23], and a means to control the inductor current $\boldsymbol{i_L}$, we are able to control the $\boldsymbol{v_C}$ output voltage, as well as react to the $\boldsymbol{v_{IN}}$ input variations.

14.0 Feedback Control Option for Good Load Regulation

From equation [13.19] we isolate the small-signal dependency of the $\boldsymbol{v_C}$ capacitor voltage on the $\boldsymbol{i_L}$ inductor current. We retain only the dependency of the capacitor voltage $\boldsymbol{v_C}$ on the feedback inductor current $\boldsymbol{i_L}$, as follows:

$$v_C = -(1-D)\frac{R_{LOAD}}{2}\frac{\left[\frac{1}{(1-D)^2}\frac{L}{R_{LOAD}}s-1\right]}{\left[\frac{R_{LOAD}C}{2}s+1\right]}i_L \qquad [14.0]$$

$$Boost(s) = Gm_{Boost} \bullet \frac{v_C}{i_L} = -\frac{(1-D)}{2}Gm_{Boost}R_{LOAD}\frac{\left[\frac{1}{(1-D)^2}\frac{L}{R_{LOAD}}s-1\right]}{\left[\frac{R_{LOAD}C}{2}s+1\right]} \qquad [14.1]$$

The objective of feedback control is to maintain the value of $\boldsymbol{V_C}$, so we can treat that quantity as quasi-static. Equation [14.1] expresses the small-signal dependency of the output voltage on the $\boldsymbol{i_L}$ inductor current. We defer discussion of how the $\boldsymbol{i_L}$ inductor current variation is developed into a signal for the feedback.

$$Boost(s) = K_{Boost}\frac{\left[\frac{1}{\varpi_Z}s-1\right]}{\left[\frac{1}{\varpi_P}s+1\right]} \qquad [14.2]$$

$$K_{Boost} = -\frac{(1-D)}{2}Gm_{Boost}R_{LOAD} \qquad [14.3]$$

$$\varpi_P = \frac{2}{R_{LOAD}C} \qquad [14.4]$$

$$\varpi_P = (1-D)^2\frac{R_{LOAD}}{L} \qquad [14.5]$$

We have the option to modify the value of $\boldsymbol{Gm_{Boost}}$ to suit our needs, but once we have chosen the inductor $\boldsymbol{L}$, capacitor $\boldsymbol{C}$, and accepted the equivalent $\boldsymbol{R_{Load}}$ and duty-cycle $\boldsymbol{D}$ ranges from the specifications, we are unable to alter the pole and zero frequencies and must compensate for the system-induced variations.

Table 14.0 Boost P-Z Summary

		Inductor = 22 µH					Capacitor = 10 µF				
		Rload = 28					Rload = 280				
V_{IN}	D	A_{Bst}	ω_P	f_P	ω_z	f_z	A_{Bst}	ω_P	f_P	ω_z	f_z
14.7	**0.48**	7.35	7.14k rps	1.14 kHz	351k rps	55.8 kHz	73.5	714 rps	114 Hz	3.51M rps	558 kHz
10.2	**0.64**	5.1	7.14k rps	1.14 kHz	169k rps	26.9 kHz	51	714 rps	114 Hz	1.69M rps	269 kHz

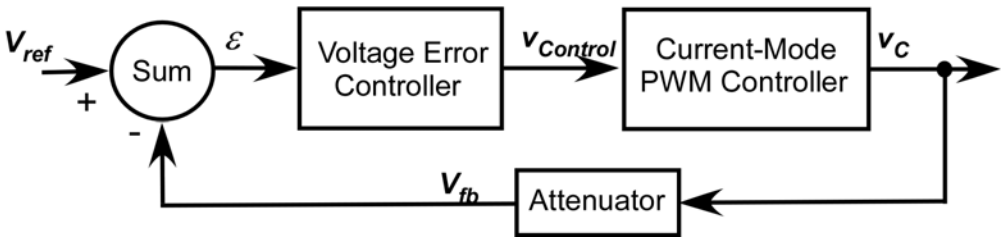

Figure 14.0 Boost Converter Small-Signal Current-Mode Controller Block Diagram

The Voltage Error Controller converts the error voltage ε into the $v_{Control}$ signal with the appropriate PZ compensation for control of the Boost PWM switching. It is the Current-Mode PWM Controller that is responsible for establishing the i_L inductor current. In that respect, ε and $v_{Control}$ are also small-signal quantities. The V_{ref} signal is typically a DC value developed from a "Bandgap" or some form of Voltage reference but not necessarily at the same level as the desired output V_C voltage. The "Attenuator" reduces the V_C voltage value so that it can be compared to the V_{ref} value and thus produces the ε error signal.

We model the Voltage Error Controller $T_{VEC}(s)$, Current-Mode PWM Controller $T_{PWM}(s)$, $Boost(s)$, and the Attenuator T_{ATTEN} as wide-bandwidth transfer functions to produce an open-loop transfer function:

$$T(s) = T_{ATTEN}\,T_{VEC}\,T_{PWM}(s)\,Boost(s) \qquad [14.3]$$

In standard form:

$$T(s) = T_{ATTEN}\,T_{VEC}(s)\,T_{PWM}(s)\,A_{Boost}\,\frac{\left[\frac{1}{\varpi_Z}s - 1\right]}{\left[\frac{1}{\varpi_P}s + 1\right]} \qquad [14.4]$$

We next examine the small-signal magnitude and phase variations of the Boost converter current control inner-loop knowing that the outer-loop for voltage control must be stable with the inner loop in place.

15.0 Boost Small-Signal Inner-Loop Bode Plot Variations

The Pole-Zero locii depend on the LC component choices made earlier to address the ripple concerns, but also depend on the operating point duty-cycle ***D*** from the turn-on instant up to the nominal worst-case operating point. In addition the pole, as well as a right-half plane zero, depend on the equivalent R_{Load} load resistor.

We do not explicitly control the selection of the duty-cycle ***D***, but rather accept it as imposed by the required operating point and as a result of the control function. Likewise, we do not explicitly control the selection of R_{Load}, rather it is the result of the DC load requirements placed on the converter. Both are "exogenous" or external quantities that we must provide a compensation scheme for Boost converter pole-zero variations in the design of the controller.

We show Bode plots of our small-signal model as we vary the exogenous duty-cycle **D** and R_{Load} load resistor variables over their expected range of operation.

Figure 16.0 below shows the expected variations in DC gain (increases with larger ***D***), as well the effect of the varying right-half plane ω_z zero adding 90° to the asymptotic phase at frequencies above the constant ω_P pole.

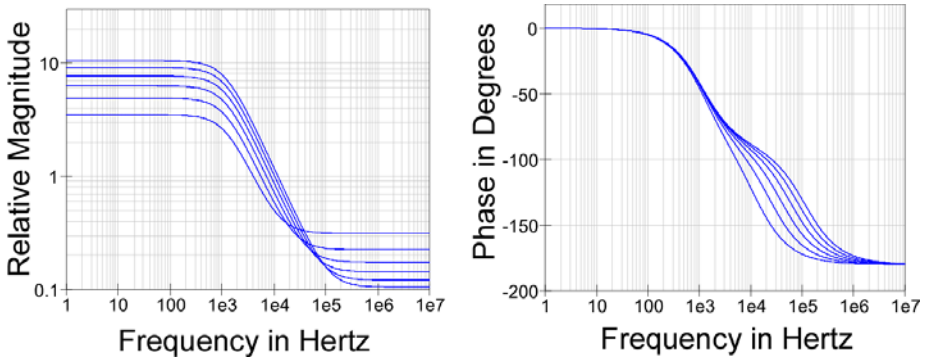

Figure 15.0 Boost Small-Signal Bode Plot: 0.25 < D <0.75, 1 Amp Load

Figure 15.0 above shows simulations with the greatest load current corresponding to R_{Load} = 28 Ω. The magnitude and phase effects of the right-half plane ω_z zero are readily apparent. We would expect to encounter such a situation whenever there are wide variations in the V_{IN} value, but R_{Load} is constant.

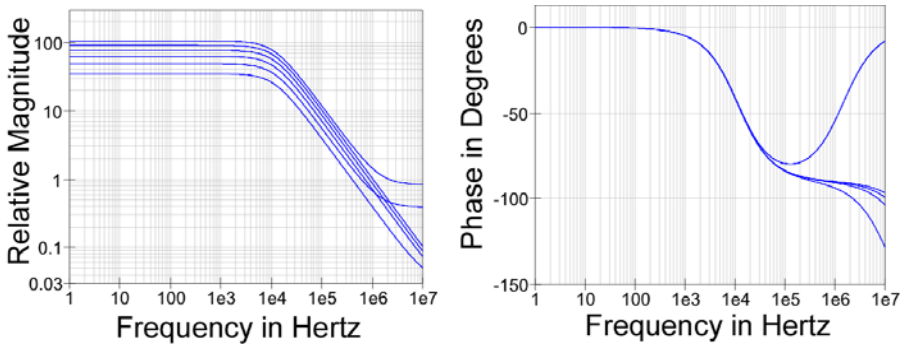

Figure 15.1 Boost Small-Signal Bode Plot: 0.25 < D <0.75, 0.1 Amp Load

Simulations in figure 15.1 are similar to those of figure 15.0, but under a minimum load condition with load current corresponding to R_{Load} = 280 Ω. The magnitude and phase effects of the right-half plane ω_z zero are readily apparent. Again, we would expect to encounter such a situation whenever there are wide variations in the V_{IN} value, but R_{Load} is light, but constant.

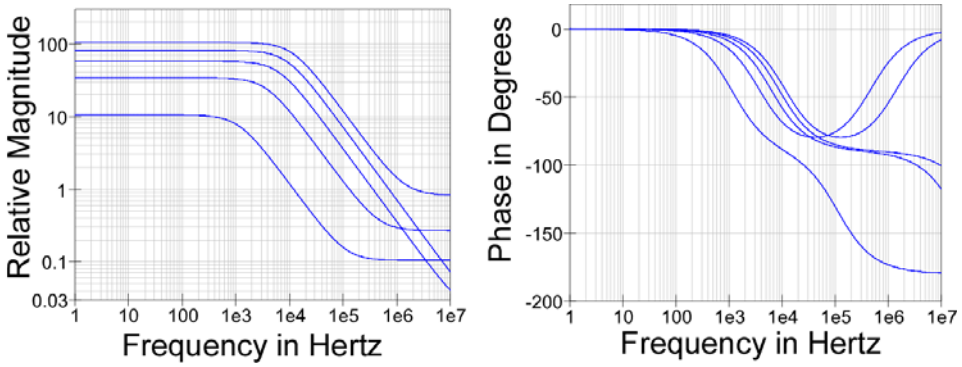

Figure 15.2 Boost Small-Signal Bode Plot: D => 0.25, 0.1 to 1 Amp Load

Figure 15.2 simulations above are performed with constant D = 0.25 and results variation in DC gain and the ω_P pole frequency. The R_{Load} variations also cause variations of the magnitude and phase of the right-half plane ω_z zero above the ω_P pole. We expect to encounter this situation with D = 0.25 whenever V_{IN} is at the high end of its range and the V_C value nearly equals the target, but R_{Load} is changing.

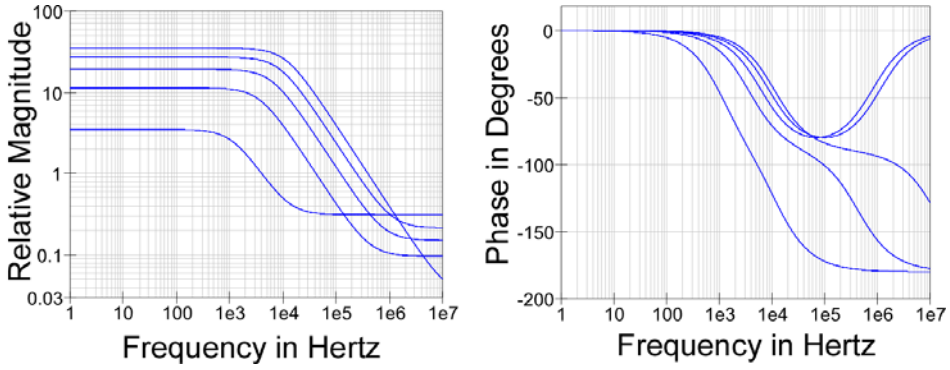

Figure 15.3 Boost Small-Signal Bode Plot: D => 0.75, 0.1 to 1 Amp Load

Figure 15.3 simulations above are similar to those of figure 15.2 but are performed with constant $D = 0.75$ and results variation in DC gain and the ω_P pole frequency. The R_{Load} variations also cause variations of the magnitude and phase of the right-half plane ω_z zero above the ω_P pole. We expect to encounter this situation with $D = 0.75$ whenever V_{IN} is at the low end of its range and the V_C value nearly equals the target, but R_{Load} is changing.

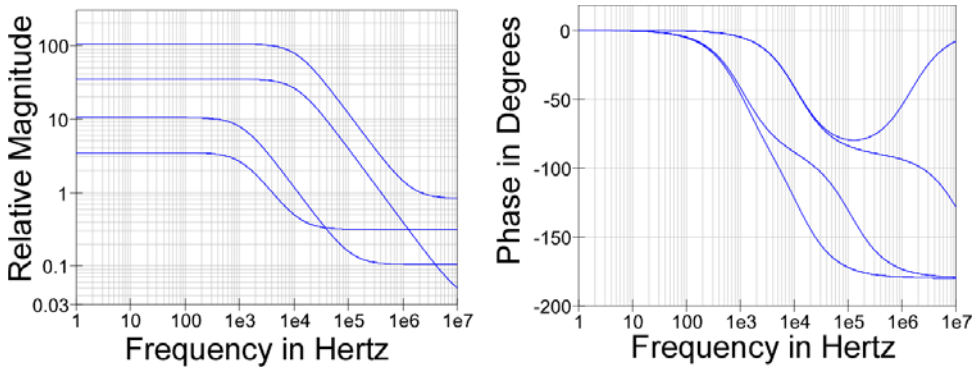

Figure 15.4 Boost Small-Signal Bode Plot: D = 0.25, 0.75; Load = 0.1, 1 Amp

Figure 15.4 shows the extreme values for the expected variations in DC gain, ω_z zero and the ω_P pole magnitude and phase ranges. The outer loop voltage feedback and PWM controller must function over this entire range of behaviors.

16.0 Discrete-Time effects of a Pulse-Width Modulator (PWM)

A Pulse Width Modulator (PWM) block adds a discrete-time sampling effect with an equivalent $T_{ZOH}(s)$ "Zero-Order-Hold" (ZOH) transfer function within the loop. State-space averaging prevents us from having an average value for a cycle of the PWM until the cycle is

complete. To model the PWM, we utilize the well-known ZOH behavior inside the loop, with an average half-cycle delay at the sampling rate, applied to each sample.

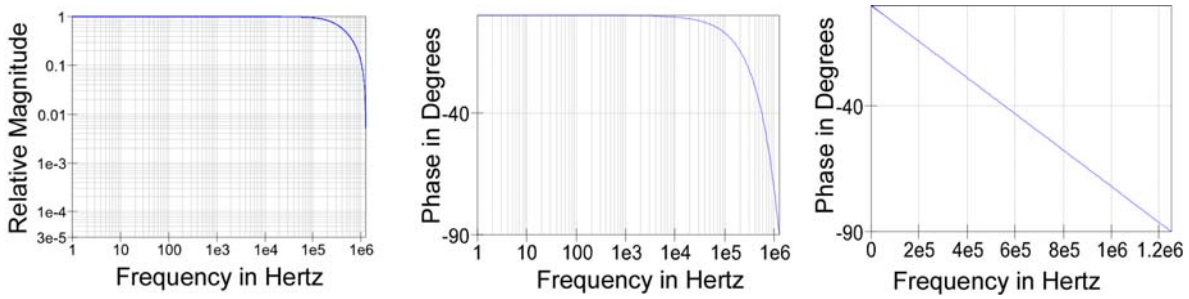

Figure 16.0 Zero-Order Hold Magnitude and Phase

A consequence introduced by the ZOH is the magnitude "notch" introduced by the ZOH at the Nyquist frequency. No magnitude information is available at the Nyquist rate. The magnitude envelope is the shape of a "cosine" with the argument equal to the ratio:

$$\left|ZOH\right| = \cos\left(2\pi \frac{f}{f_s}\right) \qquad [16.0]$$

The ZOH delay behavior also adds additional phase delay in the phase response for the loop caused by the full-cycle sampling delay. The average delay is one-half-cycle (180^o) at the sampling frequency implies half that value (90^o) at the Nyquist frequency. In figure 18.0, we show the linear phase to the right on a linear frequency scale. The $d\phi/d\omega$ is identically the constant delay. For convenience, the phase is also shown on a logarithmic frequency scale in the center of the illustration so that phase and magnitudes (from the left illustration), can more easily be associated.

Because the ZOH behavior is associated with the state-space averaging of the two switching topologies, it is best included with the small signal state-space averaged Boost model for the inner current loop and PWM. We will deal with that inclusion as we design a Pole-Zero (PZ) compensator that includes the PWM and ***Boost(s)*** into the outer loop.

17.0 Constructive Use of Switch Current Measurement in Boost Current-Mode Control

We modify the schematic of figure 8.0 to include a small $\boldsymbol{R_i}$ resistor in series with the switch ***Sw1*** in figure 17.0 as follows below:

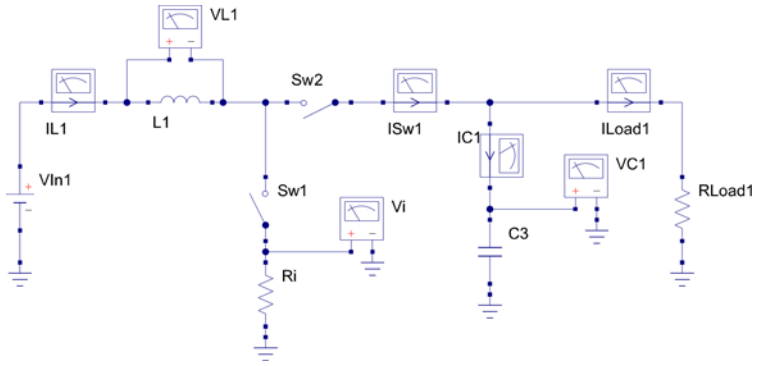

Figure 17.0 Boost Converter Schematic with R_i Resistor Added

We insert the ***R_i*** sense resistor in figure 17.0 with a value that is small enough to leave the waveforms essentially undisturbed. In figure 17.1 below, we see that the inductor current flows through the ***R_i*** resistor only during the ***DT*** interval while switch ***Sw1*** is conducting.

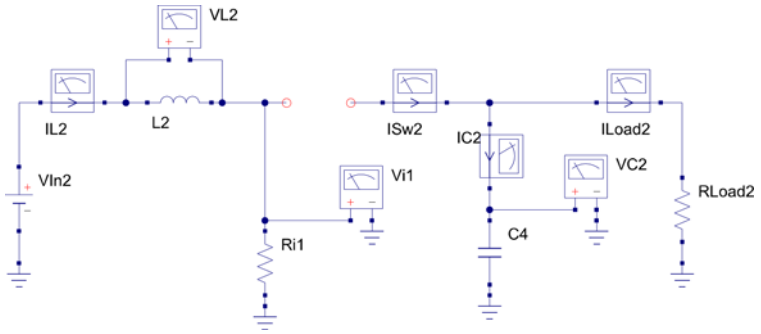

Figure 17.1 Boost Converter Schematic During the *DT* Period with R_i Resistor Added

.

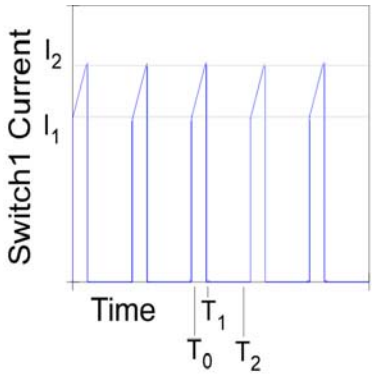

Figure 17.2 Boost Converter Sw1 and R_i Resistor Current Waveforms

We know the relationship between the output voltage V_C , the input V_{IN} voltage, and the duty cycle D, given below (in equation [1.3] and repeated here for convenience), as follows:

$$V_C = \frac{1}{1-D} V_{IN} \qquad [1.3]$$

$$D = 1 - \frac{V_{IN}}{V_C} \qquad [17.0]$$

Because the target value for output voltage V_C is fixed at 28 V, and the nominal input V_{IN} voltage range is 10.2V < V_{IN} < 14.7V, we can correlate that 0.64 > D > 0.48, and calculating expected ripple currents, as follows:

$$\Delta I_L = I_2 - I_1 = \frac{V_{IN} \bullet DT_S}{L} \qquad [17.1]$$

$$\Delta I_{L-Min} = \frac{10.2 \bullet 0.64 \bullet 400n\sec}{22uH} = 0.118Amp \qquad [17.2]$$

$$\Delta I_{L-Max} = \frac{14.7 \bullet 0.48 \bullet 400n\sec}{22uH} = 0.127Amp \qquad [17.3]$$

We know that the inductor current average value of I_L is midway between I_2 and I_1, so we can consider the peak current I_2 to represent the I_L average with an I_{Offset} of half the ripple. From equations [17.2] and [17.3], we know that the offset is bounded. The offset is expected to be between 59 mA < I_{Offset} < 64 mA, with a 5 mA uncertainty due to the operating point.

We choose a voltage comparator with a signal developed from the voltage drop across the R_i resistor to indicate that a target current has been reached and that the DT interval is complete. Further, we can use that same signal to establish a maximum current limit for the Boost converter. We employ a 50 milli-Ω resistor as a convenient value and develop 50 mV per Ampere of current. That signal can be increased by voltage amplification prior to presentation top the comparator, but that is an implementation detail left to the designer.

18.0 Constant Frequency Timing in Current-Mode Control

We provide a constant-frequency pulse-oscillator timing reference as shown in figure 18.0 from which we develop our controller timing.

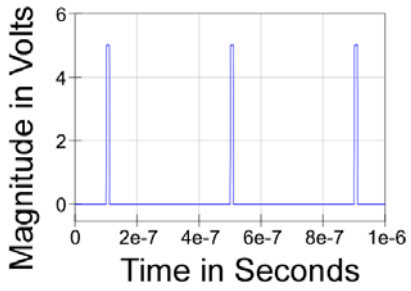

Figure 18.0 2.5MHz Pulse Oscillator Timing Reference (400 nanosecond T_S)

From the pulse oscillator, shown in figure 18.0 with a 5Volt logic-level and a 10 nano-second logic high period, we derive two delayed versions shown in figure 18.1, one designated with a T_{min} delay, and the second with a T_{max} delay relative to a T_{pulse} timing reference waveform.

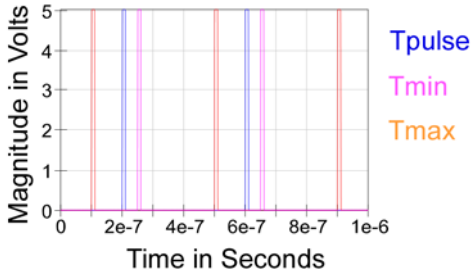

Figure 18.1 The 2.5MHz Pulse Oscillator with Two Delayed Replicas

We have shown the T_{min} with a 50 nano-second delay after the T_{pulse} timing reference waveform, and the T_{max} with a 100 nano-second delay before the T_{pulse} timing reference waveform. Implementations that control timing of these delays is possible with less than 10% uncertainty of each delay.

We will define the delay between the T_{max} and the T_{pulse} timing reference as T_{off} for reasons that will become apparent. Further, we define the delay between T_{min} and the T_{pulse} timing reference as $T_{on\text{-}Min}$ for reasons that will also become apparent.

We employ a Flip/Flop as a Pulse-Width Modulator (PWM). We initiate all PWM periods with the T_{pulse} timing reference waveform. In each PWM period the initiation called T_{Start}. The period of the PWM is controlled so that it terminates on one of three events, the waveform designated as the T_{min} waveform, the next T_{max} pulse that occurs, or a pulse that occurs between the two.

To initialize the PWM Flip/Flop, we employ a reset pulse shown in figure 16.2 that is derived from start-up logic designating that a logic high means the implementation is not ready and conversely the logic low enables the PWM Flip/Flop.

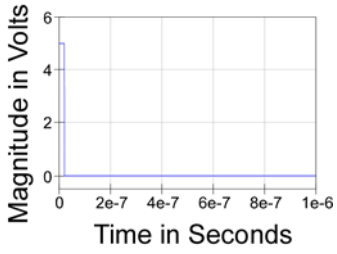

Figure 18.2 The Supervisory "Reset" Signal to Permit Timing to Commence

The PWM Flip/Flop is initialized with its output in the logic low by the supervisory signal, as shown in figure 18.2, and limited between the shortest and longest pulses displayed in figure 18.3 below.

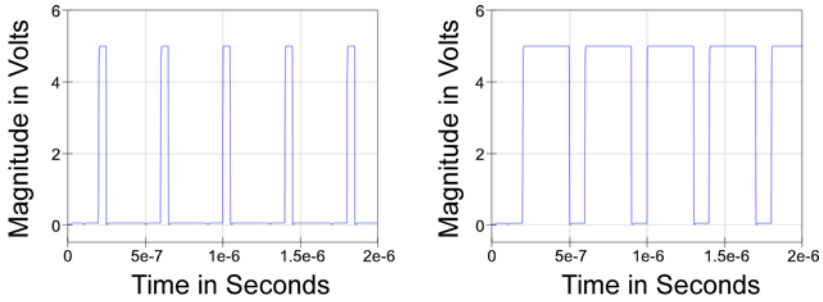

Figure 18.3 The PWM Shortest and Longest Pulses Supported at Constant T_S

The PWM Flip/Flop is initialized with its output in the logic low by the supervisory signal, as shown in figure 18.3, and limited between a shortest and longest pulse. Each PWM period begins at the T_{Start} instant.

The shortest PWM pulse occurs between that T_{Start} instant and the next following T_{min} waveform pulse. We define interval as $T_{on\text{-}Min}$ for reasons that now become apparent.

The longest PWM pulse occurs between the T_{Start} instant and the next following T_{max} pulse. We define interval as $T_{on\text{-}Max}$ for reasons that now become apparent.

We can translate the $T_{on\text{-}Min}$ and $T_{on\text{-}Max}$ time intervals into equivalent limits on the PWM duty cycle D, as follows:

$$D_{Min} = \frac{T_{on-Min}}{T_S} \qquad [18.0]$$

$$D_{Max} = \frac{T_{on-Max}}{T_S} \qquad [18.1]$$

The implementation of the delays associated with the $T_{on\text{-}Min}$ and $T_{on\text{-}Max}$ time intervals ensures that precision is easily attained.

In other implementations, the $T_{on\text{-}Min}$ and $T_{on\text{-}Max}$ time intervals may be permitted to include zero delay. Under conditions of $T_{on\text{-}Min}$ (or $T_{off\text{-}Min}$)= 0, the duty cycle is allowed to include 0% (or 100%) and the result is called "pulse-skipping." The pulse-skipping can increase efficiency under light loads, but the benefits of constant frequency are lost and as a result, Electromagnetic Interference (EMI) can easily result with pulsing modulated by the load conditions.

19.0 Current Limit Control

We introduce the current-mode control showing first the Boost converter with no current control, only the limiting effects that result from a load on the output. We then introduce a limit that establishes output conditions that are controlled by that limit and contrast the behaviors.

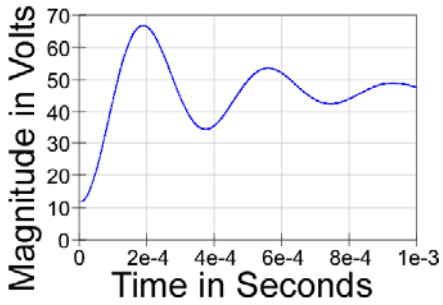

Figure 19.0 The V_C Capacitor Voltage Without Limit Control

In figure 19.0 above, we utilize only $T_{on\text{-}Max}$ time interval limit to control the PWM signal that establishes switching for the open-loop Boost converter. The response is that of a damped LC resonance as shown in the V_C output voltage in figure 19.0, the I_L inductor current in figure 19.1 below, and in the I_{Load} load current shown in figure 19.2 further below.

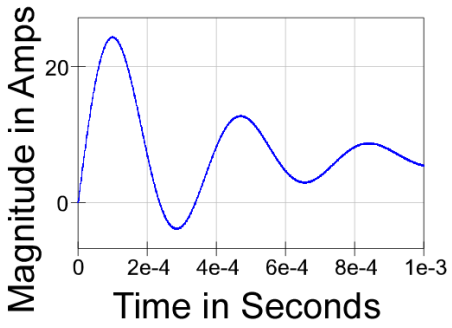

Figure 19.1 The I_L Inductor Current Without Limit Control

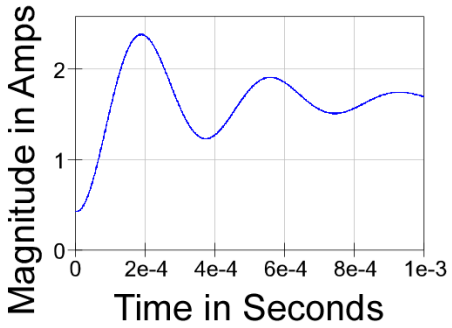

Figure 19.2 The I_{Load} Load Current Without Limit Control

The maximum duty-cycle limit imposed by the Flip-Flop PWM at D = 0.75 establishes the target V_C voltage at 1/(1-D) = 4X the V_{IN} value of 12 V (V_C => 48 V), and we see in figure 19.0 that the damped step response approaches that value. With the 28 Ω load, the I_{Load} current shown in figure 19.2 approaches the correct asymptotic value, starting from the static V_{IN}/R_{Load} initial value. Likewise, that same D = 0.75 that establishes the I_{Load} load current at (1-D) = 0.25X the I_L inductor current (I_L => 4X I_{Load}), and we see in figure 19.1 that the damped step response approaches that value.

In figure 19.3 below, we utilize the current limit comparator to terminate the PWM switching with a reset event that occurs asynchronously between the $T_{on\text{-}Min}$ and $T_{on\text{-}Max}$ time intervals.

A V_{fb} signal developed from the R_i resistor and characterized by its 50 milli-Volts per Ampere of I_L inductor current is compared to a 100 mV => 2 Ampere threshold for the I_L inductor current limit.

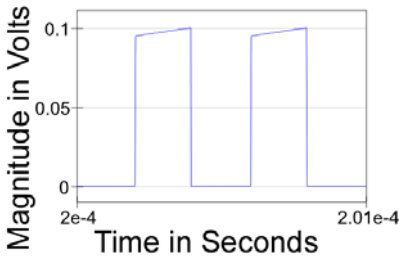

Figure 19.3 The Current Limit Comparator Terminates PWM Cycles at 100 mV

The effect of the comparator reset of the PWM in the interval during the $T_{on\text{-}Min}$ to $T_{on\text{-}Max}$ time intervals as shown in figure 19.3 is an effective means to limit the peak I_L inductor current as shown in figure 19.4 below.

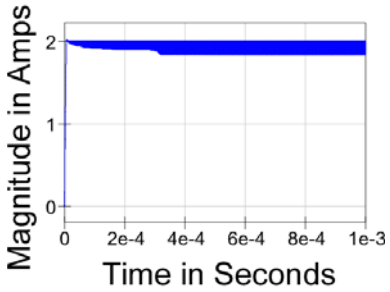

Figure 19.4 The I_L Inductor Current With PWM 2Ampere Limit Control

The current limit for the peak I_L inductor current transforms the inductor in the Boost converter into a current source. In figure 19.5 below, we see that the V_C output voltage follows the correct asymptotic trajectory for a current limited charging of the output network comprised of the 28 Ω R_{Load} and the 10 μF output capacitor

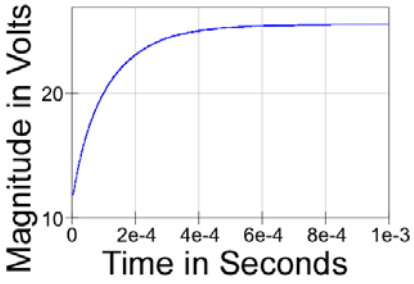

Figure 19.5 V_C Output Voltage During the Current-Limit Control

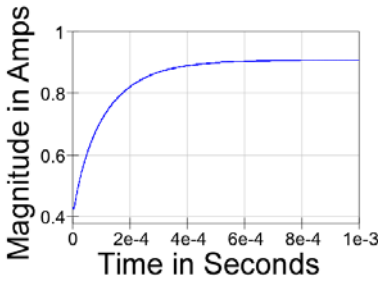

Figure 19.6 Load Current During the Current-Limit Control

As we expect, the Output current is in proportion to the output voltage and reaches the asymptotic value established by Ohm's Law but maintains the ratio to the inductor current established by the Boost converter's ***D*** duty cycle.

In figure 19.5, we see that the V_C output voltage is uncontrolled and ultimately approaches an asymptotic value that is different from the target of 28 Volts specified. It is clear, however, that we can establish another current limit and manipulate its value under feedback control to establish voltage regulation. We will establish another current limit behavior similar to that above for those instances when short-circuit, or other fault condition is encountered.

We know that the expected load current requirement is to be 1 Ampere under normal conditions. If we also allow the output capacitor to charge to the V_C output voltage target of 28 Volts during the first 400 μseconds, the charging will require an additional current given by the following:

$$I_{Charge} = C\frac{dV_C}{dt} = 10\mu F\frac{28-12}{400\mu\sec} = 0.4A \qquad [19.0]$$

The limit must be set to support current levels to the sum of the nominal load plus the charging current or 1.4A minimum from the Boost converter inductor. The limit is established on the inductor current, and not on the output directly and the I_L inductor current depends on the duty cycle as follows:

$$I_L = \frac{I_{Load}}{1-D} = \frac{1.4A}{1-0.75} = 5.6A \qquad [19.0]$$

At the maximum duty-cycle, an effective limit would be at 6 Amps on the I_L inductor current level. For the chosen R_i that occurs at a 6 X 50mV = 300 mV comparator input value.

20.0 Pulse-by-Pulse Current Control

We return to the small-signal relationship of equation [14.1], and repeated here for convenience as:

$$Boost(s) = Gm_{Boost} \bullet \frac{v_C}{i_L} = -\frac{(1-D)}{2} Gm_{Boost} R_{LOAD} \frac{\left[\frac{1}{(1-D)^2}\frac{L}{R_{LOAD}}s - 1\right]}{\left[\frac{R_{LOAD}C}{2}s + 1\right]} \qquad [14.1]$$

It is clear that the strategy of control of the inductor current controls the large-signal $\boldsymbol{V_C}$ output voltage, and the small-signal perturbations $\boldsymbol{v_C}$ around the desired operating point.

Referring to the signal developed from the $\boldsymbol{R_i}$ resistor, and characterized by the 50 milli-Volts per Ampere of $\boldsymbol{I_L}$ inductor current for the 2.5 MHz switching example, we realize that voltage value must be applied at the comparator input to obtain the peak current. The peak current differs from the average current, but is equal to the average plus half the peak-to-peak ripple current. We have shown that the ripple current is a function of the duty-cycle but not the average current, so we treat the half-ripple as an offset and retain the 50 milli-Volts per Ampere of $\boldsymbol{I_L}$ inductor current as an incremental relationship for programming current. The control is expressed as the ratio:

$$\Delta I_L = Gm_{Boost} \bullet \Delta V_{Control} \qquad [20.0]$$

$$Gm_{Boost} = \frac{\Delta I_L}{\Delta V_{Control}} = \frac{1Ampere}{0.051Volts} = 20Siemens \qquad [20.1]$$

The 20 Siemens equivalent transconductance is obtained by making incremental voltage-level changes at the input to the comparator. Because that voltage is translated by a discrete-time sampling of currents, it is not frequency independent, but rather follows previously discussed characteristics of the established small-signal $\boldsymbol{v_C/i_L}$ transfer function plus the Zero-Order Hold (ZOH) with the 2.5 MHz sampling rate, however, we can now revisit the ***Boost(s)*** transfer function as follows:

$$Boost(s) = -20 \bullet (1-D)\frac{R_{LOAD}}{2} \frac{\left[\frac{1}{(1-D)^2}\frac{L}{R_{LOAD}}s - 1\right]}{\left[\frac{R_{LOAD}C}{2}s + 1\right]} \qquad [20.2]$$

$$T(s) = T_{ATTEN} T_{VEC} T_{PWM}(s) Boost(s) \qquad [20.3]$$

Sampling using the PWM inherent Zero-Order Hold (ZOH) results in a deep notch in the transconductance at the 1.25MHz Nyquist rate. The ZOH also introduces the delay that results in the expected constant phase slope. The phase shift is most significant in the last decade before the Nyquist frequency. The ZOH phase shift, along with its magnitude effects, alters the open-loop feedback transfer function and must be considered in fast, wide-bandwidth control loops. The ZOH effects prevent feedback control at higher frequencies than or approaching the Nyquist rate.

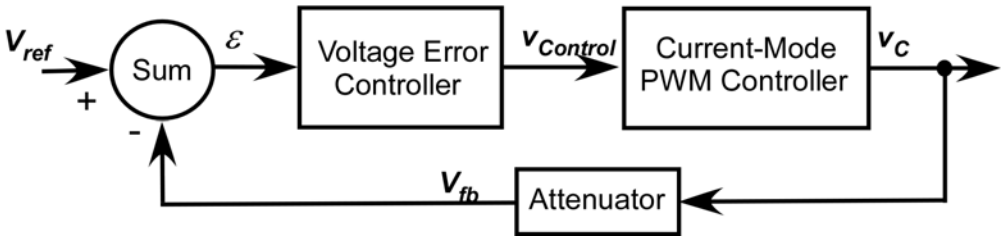

Figure 20.0 Current Control Inner/Outer Loop Feedback Structure

The transfer function from the R_i signal comparator control voltage to the output capacitor voltage is designated as $T_{Current\text{-}Control}(s)$, and is shown as the "inner-loop" as the "Current-Mode PWM Controller" in figure 20.0 above.

We return to equation [20.2] above, and include the effects of the ZOH as follows:

$$\frac{v_C}{v_{Control}} = -20 \bullet (1-D)\frac{R_{LOAD}}{2}\frac{\left[\dfrac{1}{(1-D)^2}\dfrac{L}{R_{LOAD}}s-1\right]}{\left[\dfrac{R_{LOAD}C}{2}s+1\right]}T_{ZOH} = T_{Current-Control}(s) \quad [20.4]$$

The transfer function designated as $T_{Current\text{-}Control}(s)$ is frequency dependent both from the action of the ZOH, the DC gain shift, and the zero/pole actions described earlier in the modeling.

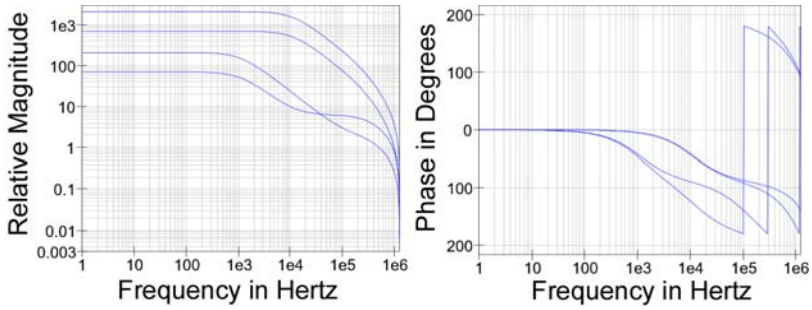

Figure 20.1 Current Control Inner Loop Bode Plots: D = 0.25, 0.75; Load = 0.1, 1 Amp

In figure 20.1, the values of R_{Load} are 280 Ω and 28 Ω, corresponding to a variation in load current over 1:10 range from 100 milli-Amperes to the full 1 Ampere required. The attenuator shown in figure 18.1 is connected directly to the V_C output and may be configured a 280 Ω resistive divider ensuring a minimum load is always present.

To complete the open-loop around an "outer" voltage feedback portion, we add the attenuator and the T_{VEC} voltage-error controller. The "Voltage Error Controller" component consists of an integrator to increase low-frequency gain, and a single pole-zero (PZ) network with the transfer function described in equation [20.5} below:

$$\frac{v_{Control}}{\varepsilon} = \frac{G_{VC}}{C_{Control}\,s}\left[\frac{\tau_{Zero}\,s+1}{\tau_{Pole}\,s+1}\right] = G_{VC} \bullet \frac{1}{C_{Control}\,s}\left[\frac{R_{Zero}C_{Zero}\,s+1}{R_{Zero}C_{Pole}\,s+1}\right] = G_{VC} \bullet Z_{VC} \quad [20.5]$$

The particular form of equation [18.4] supports an implementation consisting of a transconductance with value G_{VC}, followed by a passive network Z_{VC} at the $V_{Control}$ node.

That form of implementation supports the use of a single design that can be "tuned" connecting passive components at a single node as follows:

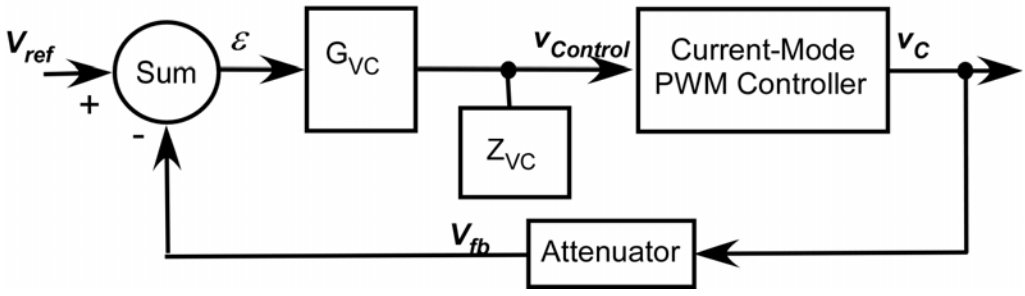

Figure 20.2 Current Control Inner/Outer Loop Feedback with G_{VC}*Z_{VC} Structure

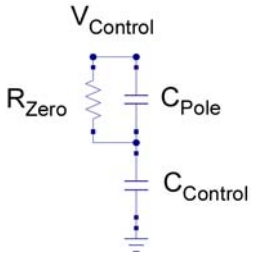

Figure 20.3 Z_{VC} Structure Schematic

$$Z_{VC} = \frac{1}{C_{Control}s}\left[\frac{R_{Zero}\left(C_{Control}+C_{Pole}\right)s+1}{R_{Zero}C_{Pole}s+1}\right] \qquad [20.6]$$

For the values of $\boldsymbol{C_{Control}}$ = 0.1µF, $\boldsymbol{C_{Pole}}$ = 10 pF, and $\boldsymbol{R_{Zero}}$ = 1000 Ω, we have a $\boldsymbol{\tau_{Zero}}$ associated with 1.6 kHz, and a $\boldsymbol{\tau_{Pole}}$ associated with 1.6 MHz. The associated $\boldsymbol{G_{VC}}$ value is 1*10-5 Siemens, which makes the $\boldsymbol{G_{VC}/C_{Control}}$ integrator pole = 16 kHz and as is shown in the Bode plots of figure 20.4 as follows:

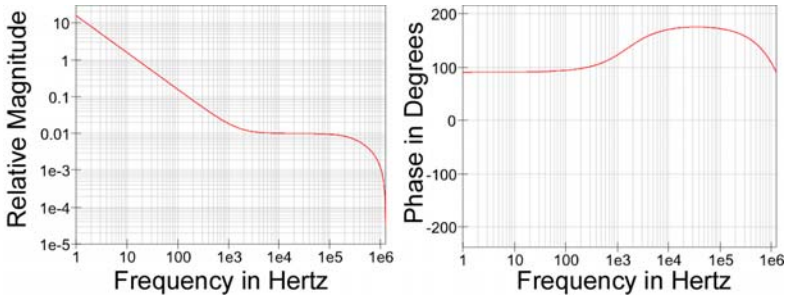

Figure 20.4 G_{VC}*Z_{VC} Structure Bode Plots with ZOH Magnitude and Phase included

Combining the $\boldsymbol{G_{VC}}$*$\boldsymbol{Z_{VC}}$ Bode Plot behavior with the Current Control Inner Loop Bode Plot behaviors, we obtain most of the open-loop behavior Bode Plots as follows:

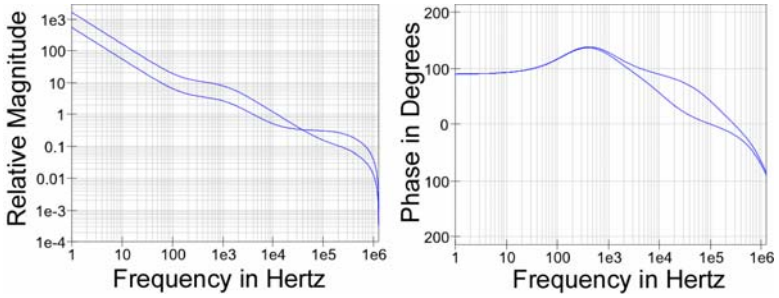

Figure 20.5 Combined Open-Loop Bode Plots: D = 0.25, 0.75; 1 Amp Load

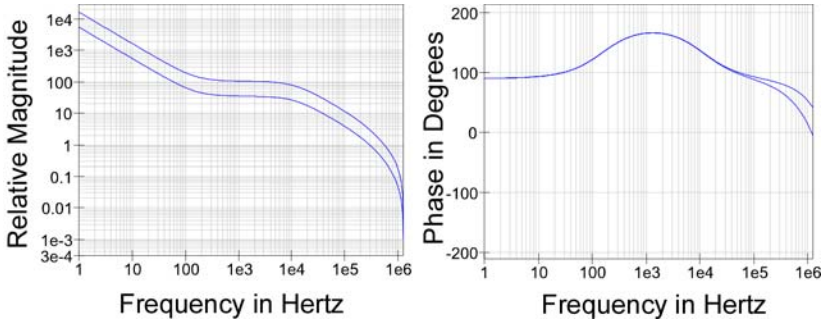

Figure 20.6 Combined Open-Loop Bode Plots: D = 0.25, 0.75; 0.1 Amp Load

The particular choice of component values at the $V_{Control}$ node, with the G_{VC} choice, produces a minimum unity-gain frequency with a 1 Ampere load of greater than 3 kHz with a phase margin greater than 70° at that frequency. If we combine a DC gain in the differential error amplifier/Sum function that is equal to the attenuator loss, there will be no effect on the stability and the loop can be closed.

21.0 Closed Loop Current Control

We close the loop shown in figure 20.2 and provide a "soft-start" ramp of the V_{ref} signal that begins at 12V and reaches the regulation V_C target of 28 Volts at 200 μsec. The "soft-start" implementation supports a controlled level of current demanded from the V_{IN} supply that is less than the ILIM maximum current limit. The soft-start feature is included for two primary reasons: first, it controls the input current resulting from initially charging the output capacitor to the operating V_C voltage, and second, it allows the feedback loop to avoid saturation and recovery during the start.

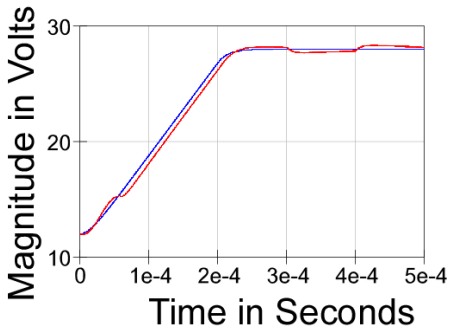

Figure 21.0 Output Voltage V_C Tracking the V_{ref} Soft-Start Ramp

Above, in figure 21.0, the reference V_{ref} control target and V_C output voltage slopes nearly match for the first 200 µsecond interval. After the V_C output voltage of 28V is reached as shown in the detail below of figure 21.1, the variation is caused by a load change to be shown later.

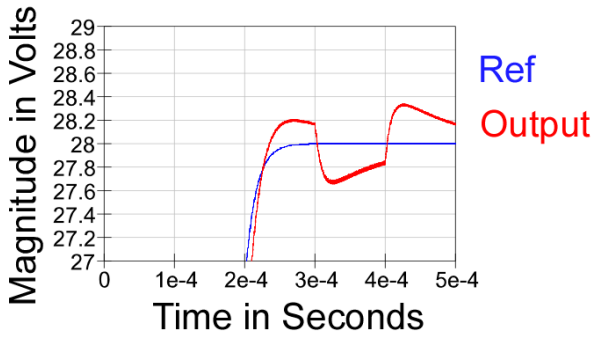

Figure 21.1 Output Voltage V_C tracking the V_{ref} Soft-Start Ramp Load-Change Detail

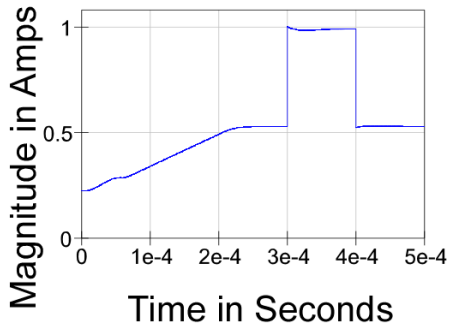

Figure 21.2 Output Voltage V_C Load-Change Current

We initiate switching with an R_{Load} = 56 Ω resistor connected as a load on the Boost converter. At the initial V_C output voltage of 12V, the load current is near 0.25 Amperes and follows the soft-start ramp of the V_C output voltage up to 28V at 200 µsec and nearly 0.5 Amperes. Beginning at the 300 µsec mark, and for an interval of 100 µsec, another 56 Ω resistor is connected in parallel making the equivalent R_{Load} = 28 Ω, and I_{Load} nearly 1 Ampere. Resistor switching is employed to make the I_{Load} changes occur as rapidly as can be expected. It is this sudden I_{Load} change shown in figure 21.2 that causes the ~1% V_C output voltage disturbance discussed above and shown in figure 21.1 above.

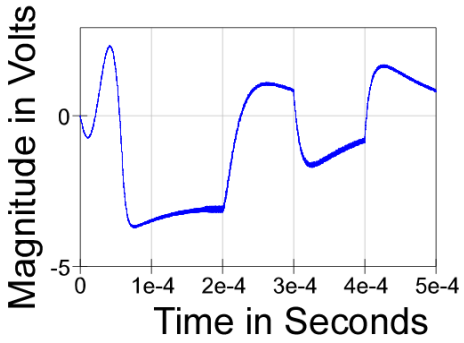

Figure 21.3 Voltage Error ε from Tracking the V_{ref}

In figure 21.3 above, we show the ε error voltage, shown with a gain of 5X between the V_{ref} signal and the resulting V_C output voltage. The initial error is caused by the $T_{on\text{-}Min}$ time constraint on the PWM duty cycle that results in a slight over-charge of the V_C output voltage for about the first 50 µsec (see figure 21.0 0). For the remaining interval to the 200 µsec mark, the error in tracking is nearly constant and proportional to the voltage required to drive the capacitor charging plus the resistor load. Following the 200 µsec mark, the integrator drives the error toward zero, except for the sudden load changes.

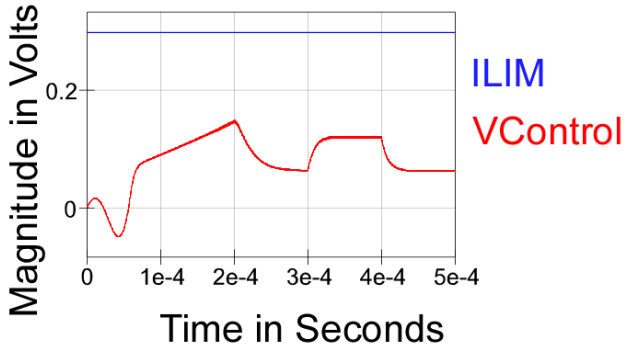

Figure 21.4 $V_{Control}$ Feedback Control Voltage for the R_i Comparator and ILIM

In figure 21.4 above, we show the $V_{Control}$ signal developed by the Pole-Zero compensation from the ε error voltage. For convenience, we also show the 300 mV ILIM current limit level that corresponds to a 6 Ampere I_L current. In figure 22.5 below, we show the R_i signal developed from the I_L current flowing through ***Sw1*** during the ***DT*** interval. We see that the $V_{Control}$ signal closely matches the R_i signal, except for the first 50 µsec caused by the $T_{on\text{-}Min}$ restraint.

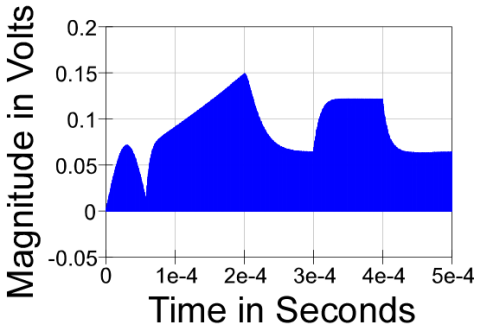

Figure 21.5 R_i Signal Caused by the I_L Current Flow through *Sw1*

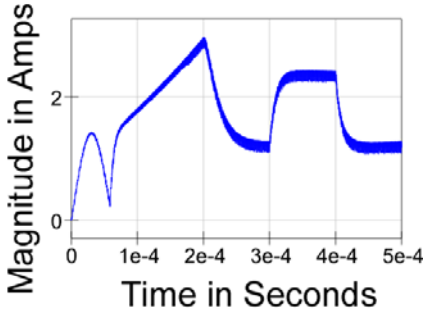

Figure 21.6 I_L Inductor Current under Current-Mode Control

22.0 Closed Loop Current Control Line Regulation

We have shown the behavior of the current-mode control with variations of load, and thus the load regulation behavior. We now introduce a 4V peak-to-peak 10 kHz sinusoidal disturbance on the V_{IN} supply as shown in figure 22.0 below to illustrate the line regulation behavior.

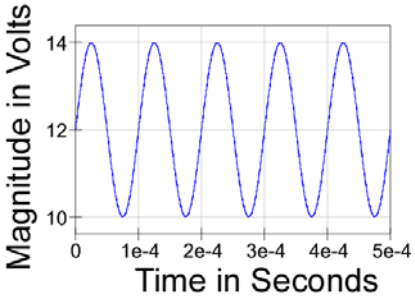

Figure 22.0 V_{IN} with 4V Peak-to-Peak 10 kHz Sinusoidal Disturbance

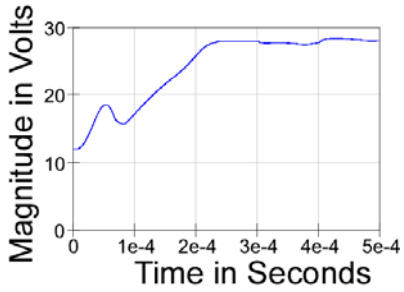

Figure 22.1 Output Voltage V_C tracking the V_{ref} Soft-Start Ramp

Large V_{IN} variations cause V_C tracking error during the first 100 µsec of the soft-start ramp, but less noticeable effects thereafter, as shown in figure 22.1 above, and the effective I_L load currents in figure 22.2 below.

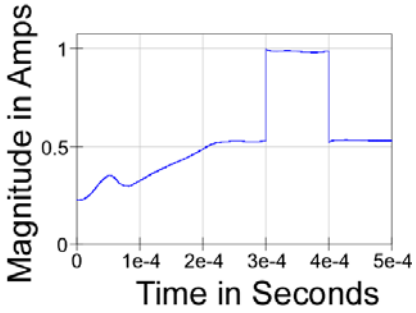

Figure 22.2 Output Voltage V_C Load-Change Current

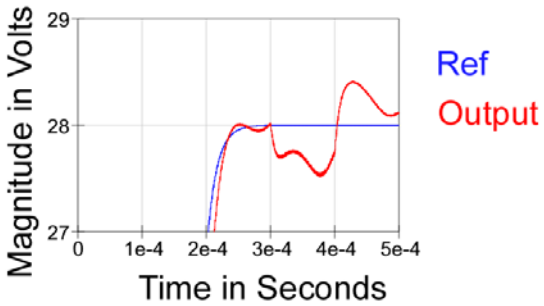

Figure 22.3 Output Voltage V_C tracking the V_{ref} Soft-Start Ramp Load-Change Detail

The large V_{IN} variations cause more noticeable V_C tracking error during load variation as shown in figure 22.3 above, with some slight sinusoidal variation in comparison to figure 21.1 without the V_{IN} disturbance. It is difficult to establish a sinusoidal peak-to-peak value of the result, but it is near 200 mV and far less than the 4V V_{IN} disturbance causing it.

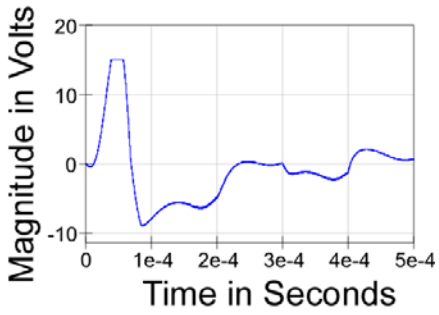

Figure 22.4 Voltage Error ε from Tracking the V_{ref}

In figure 22.4, we see that the voltage error is substantially greater that shown in figure 21.3 without a disturbance present. Much of the transient error occurs during the first 50 μsec interval and can be associated with the $T_{on\text{-}Min}$ time constraint on the PWM duty cycle.

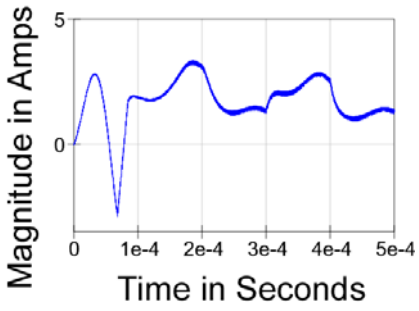

Figure 22.5 I_L Inductor Current under Current-Mode Control

In figure 22.5, we see that the inductor current shows very little discernable sinusoidal variation in the ripple current. Because we use peak current control, the relationship between the ripple current and the average current is the primary link between current control effects that result in poorer line regulation.

23.0 Slope Compensation

Current-mode control introduces instability issues if the application requires a duty-cycle greater than 50% at the nominal operating point. We have developed the example with a duty-cycle from 48% to 64% at the nominal operating point must consider the issue. In this section we show how the issue arises and one method of "Slope Compensation" for decreasing the instability, including an optimal solution that provides fast correction for small signal errors.

In figure 23.0 below, we show a detail of the inductor current with a 1 Ampere average current delivered and the implied equivalent I_{Peak} comparator level that controls the switching cycle.

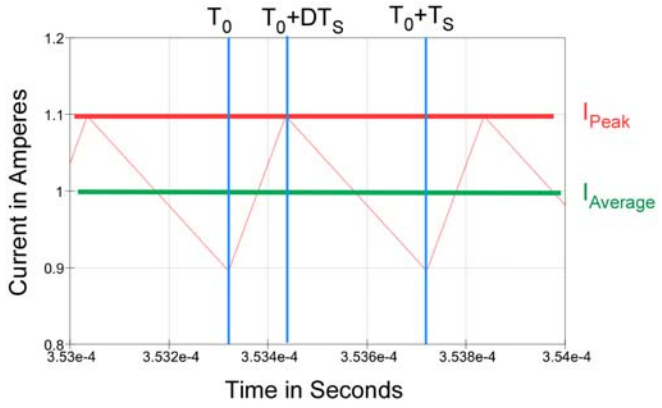

Figure 23.0 Peak Current Switching in Current-Mode Control

PWM switching is initiated by the pulse oscillator at the event marked as T_0, and every subsequent event with a T_S switching period. The PWM interval between T_0 and $T_0 + DT_S$ corresponds to the I_L inductor current rising. The crossing of the I_L inductor current through the implied equivalent I_{Peak} comparator level is the signal for switching the PWM to the remainder of the cycle indicated by the I_L inductor current falling until the next cycle initiated by the pulse oscillator at the next $T_0 + T_S$ event. The sequence of PWM events initiated by the pulse oscillator and terminated by the comparator is repeated. The implied equivalent I_{Peak} comparator level controls the cycle-by-cycle current level.

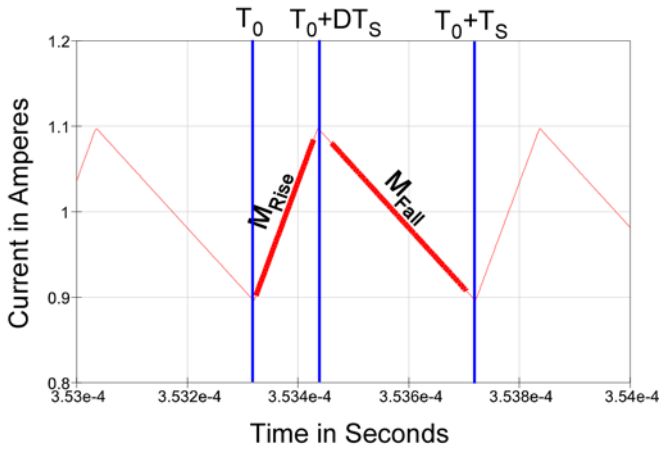

Figure 23.1 Current-Mode Control Waveform Slopes

We designate the slope of the I_L inductor rising current during the T_0 to $T_0 + DT_S$ interval as M_{Rise}, and the slope of the I_L inductor falling current during the $T_0 + DT_S$ to $T_0 + T_S$ interval as M_{Fall}, with the associated evaluations as follows:

$$M_{Rise} = \frac{V_{IN} - V_C}{L} \qquad [23.0]$$

$$M_{Fall} = \frac{-V_C}{L} \qquad [23.1]$$

Because the Buck converter voltages determine the slopes, both nominal and small-signal incremental changes can be expected during each interval.

$$M_{Rise} + m_{Rise} = \frac{V_{IN} + v_{IN} - V_C - v_C}{L} \qquad [23.3]$$

$$M_{Fall} + m_{Fall} = \frac{-V_C - v_C}{L} \qquad [23.4]$$

We find the small-signal incremental changes as follows:

$$\left(M_{Rise} + m_{Rise}\right) - M_{Rise} = m_{Rise} = \left(\frac{V_{IN} + v_{IN} - V_C - v_C}{L}\right) - \frac{V_{IN} - V_C}{L} = \frac{v_{IN} - v_C}{L} \qquad [23.5]$$

$$\left(M_{Fall} + m_{Fall}\right) - M_{Fall} = m_{Fall} = \frac{-V_C - v_C}{L} - \frac{-V_C}{L} = \frac{-v_C}{L} \qquad [23.6]$$

In equation [23.5] we find that the slope depends on the V_{IN} variations, both in large and small-signal dependencies. We have no control over the V_{IN} variations and treat the signals as exogenous and show the system response to those signals. Because the V_C output voltage is internally controlled by the feedback, we ignore the effects of that variation.

We show the remaining small-signal incremental change dependency as follows:

$$m_{Rise} = \frac{v_{IN}}{L} = \frac{dI_L}{dt} \qquad [23.7]$$

A small-signal v_{IN} results in a slope change with the same sign, but a decrease in the interval T_0 to $T_0 + DT_S$ is equivalent to a decrease in duty cycle. We have seen that our example

shows good line regulation and rejects sinusoidal variations in V_{IN} quite well. The excellent line rejection is a consequence of the operating point for the example as will become clear in the following.

For a quasi-static peak-to-peak ripple current, we show that in a single cycle:

$$m_{Rise} = \frac{I_{L-Peak-to-Peak}}{\Delta T} \qquad [23.8]$$

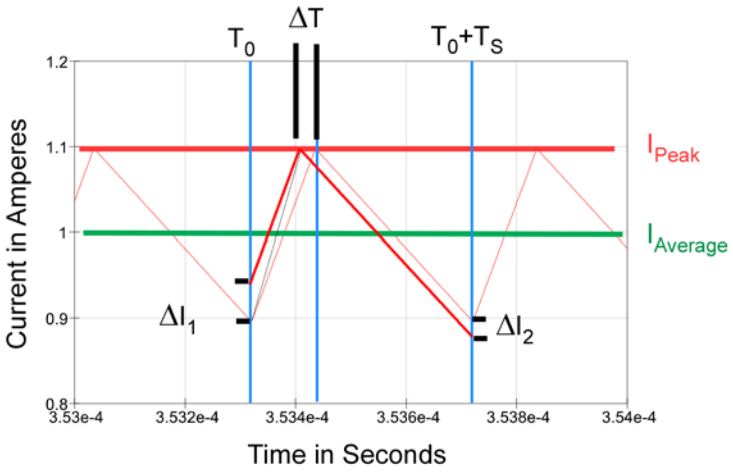

Figure 23.2 Current-Mode Control Incremental Equivalents

In figure 23.2, we see that an incremental increase in the m_{Rise} slope produces a ΔT incremental decrease in the $T_0 + DT_S$ interval, as well as a ΔT incremental increase in the $T_0 + DT_S$ to $T_0 + T_S$ interval. If we interpret the increase in the m_{Rise} slope as an isolated event, the momentary event is equivalent to a single instantaneous incremental change ΔI_1 at the T_0 event.

$$\left|M_{Rise}\right| = \left|\frac{\Delta I_1}{\Delta T}\right| \qquad [23.9]$$

In a similar fashion, the ΔT incremental increase in the $T_0 + DT_S$ to $T_0 + T_S$ interval produces an incremental current ΔI_2 at the $T_0 + T_S$ event.

$$\left|M_{Fall}\right| = \left|\frac{\Delta I_2}{\Delta T}\right| \qquad [23.10]$$

$$\left|\frac{M_{Rise}}{\Delta I_1}\right| = \left|\Delta T\right| = \left|\frac{M_{Fall}}{\Delta I_2}\right| \qquad [23.11]$$

$$\left|\frac{\Delta I_2}{\Delta I_1}\right| = \left|\frac{M_{Fall}}{M_{Rise}}\right| \qquad [23.12]$$

Except for the difference in sign, the ΔI_2 at the $T_0 + T_S$ event is similar to the single instantaneous incremental change ΔI_1 at the T_0 event. The relationship between the slopes determines whether the incremental current magnitude is reduced or grows in following cycles.

We refer to figure 23.1 with a constant peak-to-peak ripple current to show:

$$DT_S M_{Rise} + (1-D)T_S M_{Fall} = 0 \qquad [23.13]$$

$$DM_{Rise} = -(1-D)M_{Fall} \qquad [23.14]$$

$$\frac{D}{1-D} = -\frac{M_{Fall}}{M_{Rise}} \qquad [23.15]$$

$$\left|\frac{D}{1-D}\right| = \left|\frac{M_{Fall}}{M_{Rise}}\right| = \left|\frac{\Delta I_2}{\Delta I_1}\right| \qquad [23.16]$$

After a number "N" of cycles, we have:

$$\left|\Delta I_N\right| = \left|\frac{D}{1-D}\right|^N \left|\Delta I_1\right| \qquad [23.17]$$

We see that for $D = 0.5$, an incremental disturbance persists, and for $D > 0.5$, it grows without bound.

To remove the effects of disturbances, we add a periodic "Slope Compensation" sawtooth waveform to the I_{Peak} comparator reference signal as shown in figure 21.3 below:

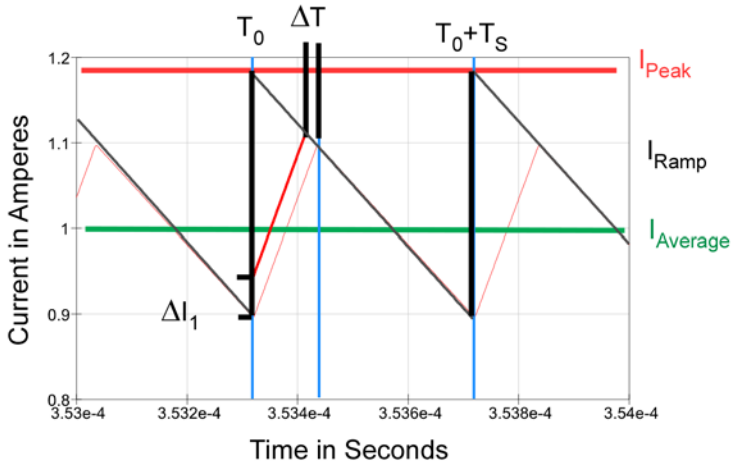

Figure 23.3 Current-Mode Control with Slope Compensation Sawtooth

With the addition of the sawtooth waveform, the $\boldsymbol{I_{Peak}}$ comparator level is initiated at a higher level and the periodic sawtooth "Slope Compensation" waveform is subtracted, decreasing the $\boldsymbol{I_L}$ peak intersection as shown. The disturbance current causes an intersection at a new time, produces a new incremental $\boldsymbol{\Delta T}$, but because the periodic sawtooth "Slope Compensation" waveform is chosen with its slope identical to the $\boldsymbol{M_{Fall}}$ slope, there is no resulting $\boldsymbol{\Delta I}$ disturbance after the first cycle.

$$\Delta I_N = \left[-\frac{M_{Fall} - M}{M_{Rise} + M} \right]^N \Delta I_1 \qquad [23.18]$$

The parameters in equation [23.18] include the equivalent magnitudes of the slope of the compensation sawtooth M, as well as the $\boldsymbol{I_L}$ slopes. Magnitudes are used throughout to remove sign confusions arising from the rising and falling slopes.

24.0 Closed Loop Slope Compensation Comparison

We modified the structure discussed in section "**21.0 Closed Loop Current Control**" to present detailed PWM behavior without slope compensation, and then again with slope compensation. The range of duty cycle from 0.48 to 0.64 required by this application must employ slope compensation for values above 0.5, but the magnitude of the slope compensation is relatively small due to the limited upper range encountered.

We have chosen a set of intervals from 2 μsec before the load increases at 300 μsec and also before the load decreases at 400 μsec. We have presented the effects until 4 μsec after the load transitions have occurred for comparisons.

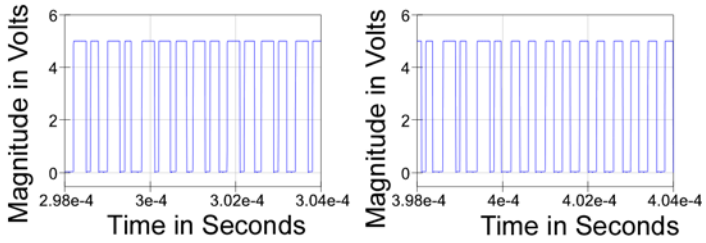

Figure 24.0 Current-Mode Control PWM without Slope Compensation Sawtooth

In figure 24.0, we note a long-short pattern that we expect from the instability arising with the duty cycle in excess of 0.5 at both transitions, although the load decrease seems to have a period of relative constant PWM pulse width following the decrease in load current.

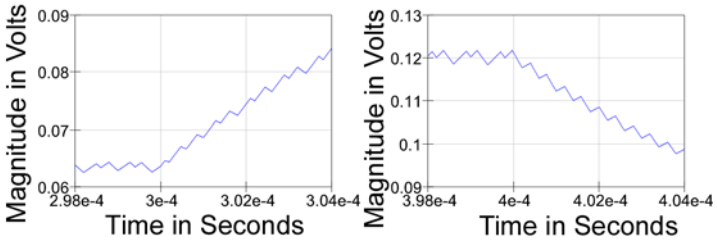

Figure 24.1 Feedback $V_{Control}$ Signal without Slope Compensation Sawtooth

In figure 24.1, we note a varying threshold on the $V_{Control}$ that we expect from the instability arising with the duty cycle in excess of 0.5 at both transitions, although the load decrease has made the variation more regular following the decrease in load current.

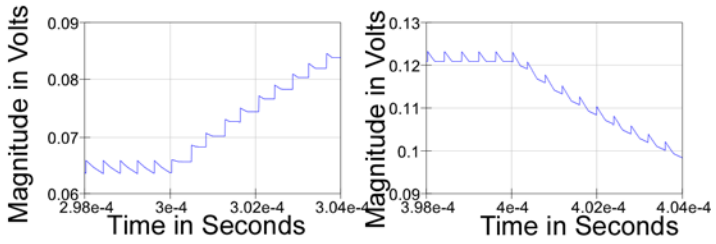

Figure 24.2 Feedback $V_{Control}$ Signal with Slope Compensation Sawtooth

In figure 24.2, we note the addition of a small slope compensation sawtooth waveform at the beginning of each PWM interval and ending when the comparator threshold causes the end of the PWM cycle. The waveform is much more regular in the $V_{Control}$ signal, but the important behavior is more obvious in figure 24.3 below.

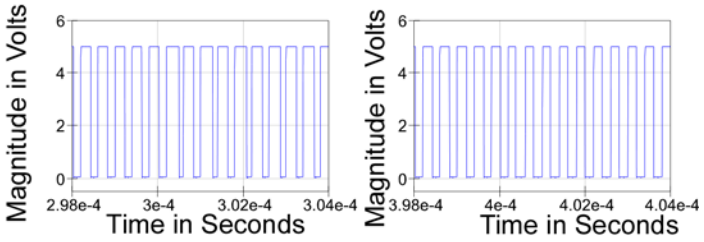

Figure 24.3 Current-Mode Control PWM without Slope Compensation Sawtooth

In figure 24.3, we note the absence of the long-short pattern that we observed above. The PWM duty cycle varies in a much smoother pattern following each load transition

25.0 Summary and Conclusions

We have introduced a constant frequency Switchmode Boost power conversion topology. The selection of appropriate inductor and capacitor values were discussed, considering the frequency of operation and other design parameters.

We analyzed the topologies for two states of switching and produced a state-space averaged model. We extracted a small-signal model and developed a linear model to examine potential stability issues. We included Zero-Order Hold (ZOH) effects of the discrete-time nature of the switch within the control loop, including extra phase contributions and the "notch" behavior near the Nyquist frequency. We designed a Pole-Zero (PZ) compensator necessary to stabilize the open-loop characteristics of the converter with disparate operating points.

We introduced a pulse oscillator timing reference and delay functions to establish minimum and maximum time intervals for a Flip-Flop constant-frequency Pulse-Width Modulator (PWM) controller and introduced it into the feedback loop.

A method for constructive use of a resistor in the switching path was employed for current monitoring. We introduced the peak-threshold current control in the open-loop model to illustrate a current-limit function, and then developed that control into the pulse-by-pulse peak current-mode control comparators and used them to control the duration of the PWM for voltage feedback.

We developed the feedback conditions for frequency-domain, small-signal, stability in the open-loop model and included a Pole-Zero (PZ) compensator for good margins. We introduced the Zero-Order-Hold (ZOH) effects of the inherent sampling caused by cycle-by-cycle control and included those effects in the (PZ) compensator. The loop was closed and a

"soft-start" capability added to avoid current-limiting during startup. Line and load regulation was shown for the example as well as transient load recovery. Finally, the need for "Slope Compensation" in some designs was discussed and a means for adding it shown.

A more complete design would also consider development of voltage reference components, power switching components, amplifier designs, supervisory startup circuits, component costs, and efficiency effects of component selection, but are beyond the scope of this course. The material covered should enable a working engineer to construct a stable Boost converter using current-mode control.

