Switchmode Boost Power Converter Using Voltage-Mode Control©

By

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1.0 Switchmode Boost Power Converter Introduction and Basic Model

This course develops models of the Boost converter with duty cycle control. Basic operation, a practical set of examples, and large/small signal models are discussed. Considerations for feedforward control to address line regulation and feedback control to address load regulation of the converter are included.

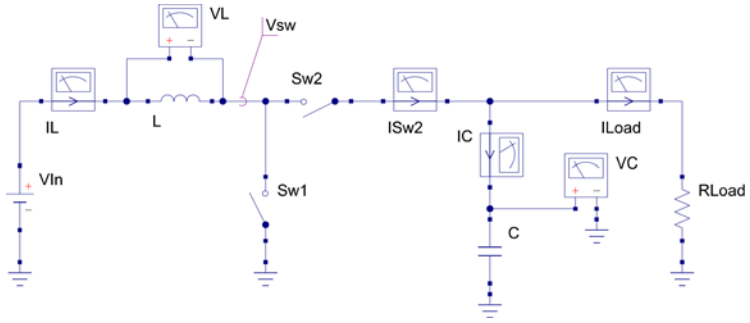

Figure 1.0 Ideal Boost Converter Schematic

We develop a constant frequency, continuous current Boost converter design, with the switching period defined below in figure 1.1 by $T_2 - T_0 = T$. The converter has two conducting states defined by periods $T_1 - T_0 = DT$ and $T_2 - T_1 = (1 - D)T$, corresponding to the two switching states. The V_{sw} node is connected using S_{w1} to ground with the duty cycle D, and a complement controlled synchronous switch S_{w2} is applied to connect the V_{sw} node to the output network during the remaining $(1 - D)$ portion of the period.

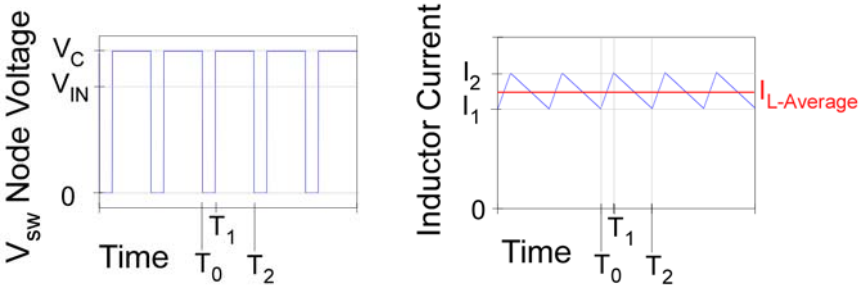

Figure 1.1 Boost Converter Inductor Operating Waveforms

The inductor cannot support a DC voltage difference across its terminals. Instead, any short-term V_L voltage difference results in a constant rate of change of current I_L through the inductor. With some V_C voltage on the capacitor, the inductor has a voltage difference V_{IN} applied during the DT interval and $V_C - V_{IN}$ applied during the $(1 - D)T$ interval.

We can equate the volt-second products and keep a zero voltage average as:

$$V_{IN}DT - (V_C - V_{IN})(1-D)T = 0 \qquad [1.0]$$

$$V_{IN}D = (V_C)(1-D) - (V_{IN})(1-D) \qquad [1.1]$$

$$V_{IN}D + V_{IN}(1-D) = V_C(1-D) \qquad [1.2]$$

$$V_C = \frac{1}{1-D}V_{IN} \qquad [1.3]$$

Equation [1.3] provides the property of the Boost converter that shows that a larger output voltage $\boldsymbol{V_C}$ can be obtained from the input $\boldsymbol{V_{IN}}$ voltage by controlling the duty cycle $\boldsymbol{D}$.

2.0 Switchmode Boost Power Converter Input/Output Current Waveforms

As shown in figure 1.1 above, the $\boldsymbol{I_{IN}}$ input current the inductor current, and is continuous and non-zero. However, as shown in figure 2.0 below, the $\boldsymbol{S_{w1}}$ current to ground during the $\boldsymbol{T_1 - T_0 = DT}$ intervals, as well as the $\boldsymbol{S_{w2}}$ current to the output voltage $\boldsymbol{V_C}$ during the $\boldsymbol{T_2 - T_1 = (1-D)T}$ intervals are both discontinuous.

The $\boldsymbol{I_{LOAD}}$ output current is continuous and flows through the $\boldsymbol{R_{LOAD}}$ resistor as a combination of currents from the $\boldsymbol{S_{w2}}$ current and the capacitor. Because the capacitor cannot support a continuous current, but does sink/source AC and transient currents, the average current to the load is identical to the average $\boldsymbol{S_{w2}}$ current.

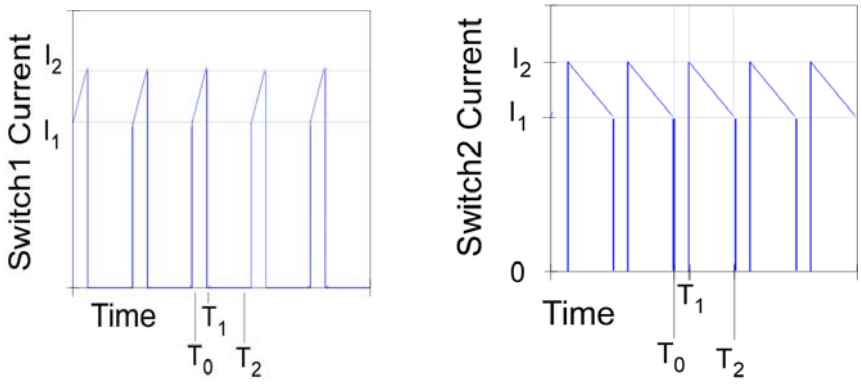

Figure 2.0 Boost Converter Switch Current Waveforms

The average input current is identical to the $I_{L\text{-}Average}$ current. The conducting S_{w2} current is the inductor current and has the same $I_{L\text{-}Average}$ current during its ON-state, but because it is non-zero only during $(1-D)T$ intervals, its average value is $(1-D)I_{L\text{-}Average}$ over each entire period. Consequently, the average I_{LOAD} output current is also equal to the same $(1-D)I_{L\text{-}Average}$ over each entire period.

3.0 Switchmode Boost Power Converter Input/Output Power and Efficiency

We can calculate the average input power from the product of the input V_{IN} supply times the average I_L input current as follows:

$$P_{IN} = V_{IN} \bullet I_{L-Average} \qquad [3.0]$$

Similarly, we can calculate the average output power from the product of the output V_C output times the average I_{LOAD} output current as follows:

$$P_{OUT} = V_C \bullet I_{LOAD} = V_C \bullet (1-D) I_{L-Average} \qquad [3.1]$$

If we insert equation [1.3] for the value of V_C in terms of the V_{IN} input voltage into equation [3.1], we find that the input and output average power levels are identical:

$$P_{OUT} = V_C \bullet I_{LOAD} = \frac{1}{1-D} V_{IN} \bullet (1-D) I_{L-Average} = P_{IN} \qquad [3.2]$$

The indicated 100% efficiency is not correct because we have not accounted for losses in the switching elements, or the non-ideal practical components that we must use to implement the design, however, very high efficiencies are achievable, often exceeding 90% efficiency in a practical design.

It is the high efficiency of the switch-mode power converters that accounts for the interest, despite the complexities of the design and control means required to implement a practical design.

4.0 Output Load Current Range

The worst-case, highest current is determined by the smallest R_{LOAD} value, and in turn, the highest I_{LOAD} value. The current handling capacity of the switching devices must be sufficient to support switching the maximum I_{LOAD} value with sufficient speed to support the switching for both DT and $(1-D)T$ periods.

The maximum value that the R_{LOAD} resistor may attain may be constrained to determine a minimum I_{LOAD} value. A minimum current value may be employed to ensure continuous load current, and to ensure stability requirements

5.0 Input/Output Ripple Current Effects in Component Value Selection

We see from equation [1.3] that the frequency does not enter directly into the relationship between the input voltage and the output voltage, only the duty cycle ***D*** is directly involved. In figure 1.1, we also see that the inductor current forms a triangular waveform between the I_2 peak current, and the I_1 valley current. The triangular peak-to-peak current is defined to be a "ripple current," and is an AC waveform superimposed on the average or DC inductor current.

From the fundamental differential equation description of the behavior of an ideal inductor we have:

$$V_L = L \bullet \frac{dI_L}{dt} \qquad [5.0]$$

For a regime with relatively short times, relatively large inductor values, and relatively small voltages, we can approximate the relationship with line segments as follows:

$$V_L = L \bullet \frac{\Delta I_L}{\Delta t} \qquad [5.1]$$

And in more useful form:

$$\Delta I_L = I_2 - I_1 = \frac{V_L \bullet \Delta t}{L} \qquad [5.2]$$

From equation [5.2], we see that the "volt*second product" of the applied waveform can be used to determine the triangular "ripple" current between the I_2 and I_1 limits. To ensure continuous operation, we implement the design so that I_1 remains non-zero. We select an inductor value large enough to support the "volt*second product" and satisfy the remaining design parameters.

From the fundamental differential equation description of an ideal capacitor we have:

$$I_C = C \bullet \frac{dV_C}{dt} \qquad [5.3]$$

There are two distinct time intervals for capacitor currents, the ***DT*** interval and the ***(1-D)T*** interval. During the DT interval, the capacitor is discharging into the R_{Load} load resistor

alone, and the discharge follows the familiar exponential with a $\boldsymbol{CR_{Load}}$ time constant. During the ***(1-D)T*** interval, however, there is also added the charging current through the $\boldsymbol{S_{w2}}$ switch. The waveform during each interval can obtained by solving the differential equation explicitly, but detailed waveshape information is not necessary, only the peak-to-peak voltage ripple. We use only the discharge portion of the cycle, during the ***DT*** interval to solve as follows:

$$\Delta V_C = V_C\left(1 - e^{-\frac{DT_S}{CR_{Load}}}\right) \qquad [5.4]$$

Using a "straight-line" approximation and taking the derivative of equation for the slope of the discharge line, we have:

$$\Delta V_C \cong -\frac{DT_S}{CR_{Load}} V_C \qquad [5.5]$$

Equation [5.4] offers a value for the peak-to-peak ripple voltage that can be expected to be caused by the choice of capacitor value and time interval, but it is probably more useful expressed as the ratio:

$$\frac{\Delta V_C}{V_C} \cong -\frac{DT_S}{CR_{Load}} \qquad [5.5]$$

Additional non-ideal parasitic components are needed to describe the power lost in the inductor and capacitor.

6.0 Input/Output Voltage Range Considerations

Practical applications require that we produce a controlled value for $\boldsymbol{V_C}$ over a range of input voltage $\boldsymbol{V_{IN}}$ values.

For instance, automotive applications may require a nominal 12V $\boldsymbol{V_{IN}}$ operation, but be expected to function nominally under a low battery condition below 10V, and also operate with transient $\boldsymbol{V_{IN}}$ values in excess of 52V for a few milliseconds in the case of "load-dump" of highly inductive DC motor and solenoid devices connected to that same battery/alternator system. The $\boldsymbol{V_{IN}}$ range can be >5:1 for some automotive applications.

Similarly, "line-powered" applications may be expected to function correctly with common switching circuitry when powered from 110/220V mains sources. The line-powered ranges

may be ~85V from the low-line 110V source, but also as higher than 365V under high-line 220V sourcing. The V_{IN} range can be >4.5:1 for some "line-powered" applications.

Although many applications require a fixed output voltage, there are also applications that require a user-programmed output voltage also, often over a considerable range of values.

The capacitor must withstand the highest expected output voltage under both nominal and transient conditions.

The ratio of the smallest output voltage to the highest input voltage determines the smallest nominal value of duty-cycle required. Likewise, the ratio of the highest output voltage to the lowest input voltage determines the largest value of duty-cycle required.

7.0 Switchmode Boost Power Converter Line/Load Regulation Introduction

Practical applications typically require that we provide a controlled value for V_C despite changes in the input voltage V_{IN}. The term "line regulation" is used to describe the resulting effect of that control effort.

Also, practical applications require that we provide a controlled value for V_C despite changes in the load current I_{LOAD}. The term "load regulation" is used to describe the resulting effect of that control effort.

Practical applications use a combined strategy for controlling the duty cycle dependent on both the V_{IN} and the V_C values. That part of the control that uses the V_{IN} value to control the duty cycle is called a "feedforward" control mechanism. That part of the controller that uses the V_C value to control the duty cycle is called a "feedback" control mechanism.

To facilitate each form of control, a detailed small-signal model is developed so that the stability and performance of the control can be determined. If feed-forward control is utilized, it is designed later and applied to the system to modify the model behavior after feedback is developed. However, the feedforward control lessens the changes in V_C that the feedback must deal with, making the feedback design less demanding. It is the feedback control that requires a small-signal model to determine gain and phase margins, as well as any compensation required to stabilize the closed loop behavior.

8.0 Switchmode Boost Power Converter Duty-Cycle Control Model

The Boost converter model is described using two state variables: the inductor current I_L and the capacitor voltage V_C. The input voltage V_{IN} and the load resistance R_{LOAD} are retained to express the input and output dependencies for line and load regulation.

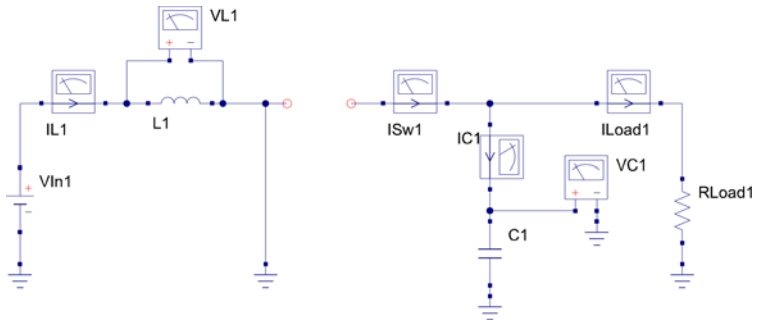

Figure 8.0 Boost Converter Schematic During the *DT* Period

Modeling begins with the topology defined in figure 8.0 during the ***DT*** interval with the grounding switch S_{w1} conducting and S_{w2} OFF. We use Kirchoff's Voltage Law (***KVL***) around the loop including V_{IN}, and ***L***, and Kirchoff's Current Law (***KCL***) at the node defined by the V_C voltage, to write two defining equations:

$$V_{IN} = V_L \qquad [8.0]$$

and

$$0 = I_{LOAD} + I_C \qquad [8.1]$$

Because V_L, I_{LOAD}, and I_C are not the chosen state variables, we rewrite the equations in terms of the state variables, and use the Laplace "***s***" operator to obtain the equations:

$$V_{IN} = LsI_L \qquad [8.2]$$

and

$$0 = \frac{V_C}{R_{LOAD}} + CsV_C \qquad [8.3]$$

We rewrite equations [8.2] and [8.3] into differential equation form, as follows:

$$sI_L = \frac{1}{L}V_{IN} \qquad [8.4]$$

and

$$sV_C = -\frac{1}{CR_{LOAD}}V_C \qquad [8.5]$$

We define a state vector composed of the two state variables:

$$X = \begin{vmatrix} I_L \\ V_C \end{vmatrix} \qquad [8.6]$$

We then express the two equations in matrix form using the state vector and build the state matrix as the expression of the two simultaneous equations. It is a matrix differential equation with the derivative of the state vector ***Xs***, expressed in terms of the state vector ***X*** itself and the $\boldsymbol{V_{IN}}$ input voltage:

$$Xs = \begin{vmatrix} 0 & 0 \\ 0 & -1/CR_{LOAD} \end{vmatrix} X + \begin{vmatrix} 1/L \\ 0 \end{vmatrix} V_{IN} \qquad [8.7]$$

The matrix differential equation [8.7] describes the behavior of the Boost converter during the time ***DT*** that the input supply is connected through the closed $\boldsymbol{S_{w1}}$ switch.

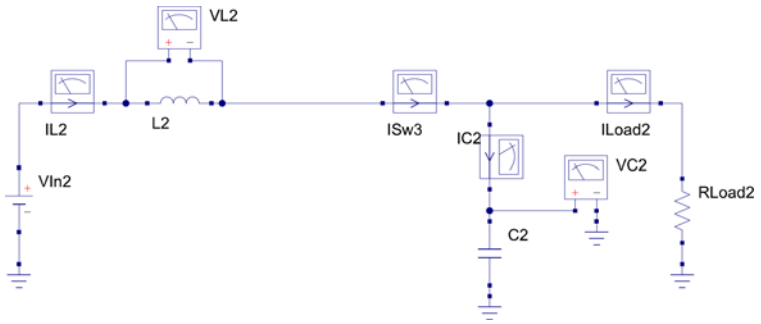

Figure 8.1 Boost Converter Schematic During the (1-*D*)*T* Period

We continue modeling with the topology defined in figure 8.1, with conduction through the synchronous switch during the ***(1-D)T*** interval, again using ***KVL*** and ***KCL*** to write two modified defining equations:

$$V_{IN} = V_L + V_C \qquad [8.8]$$

and

$$I_L = I_{LOAD} + I_C \qquad [8.9]$$

As before, we rewrite the defining equations:

$$V_{IN} = LsI_L + V_C \qquad [8.10]$$

and

$$I_L = \frac{V_C}{R_{LOAD}} + CsV_C \qquad [8.11]$$

We write equations [8.10] & [8.11] into explicit differential equation form, as follows:

$$sI_L = -\frac{1}{L}V_C + \frac{1}{L}V_{IN} \qquad [8.12]$$

and

$$sV_C = \frac{1}{C}I_L - \frac{1}{CR_{LOAD}}V_C \qquad [8.13]$$

Using the state vector as previously defined, we express the new matrix differential equation as follows:

$$Xs = \begin{vmatrix} 0 & -1/L \\ 1/C & -1/CR_{LOAD} \end{vmatrix} X + \begin{vmatrix} 1/L \\ 0 \end{vmatrix} V_{IN} \qquad [8.14]$$

9.0 Switchmode Buck Power Converter State-Space Average Model

Following the practice of state-space averaging, we sum ***D*** times the component matrix in equation [8.7] plus ***(1-D)*** times the component matrix in equation [8.14] to provide the state-space averaged equations:

$$Xs = D\begin{vmatrix} 0 & 0 \\ 0 & -1/CR_{LOAD} \end{vmatrix} X + D\begin{vmatrix} 1/L \\ 0 \end{vmatrix} V_{IN} + (1-D)\begin{vmatrix} 0 & -1/L \\ 1/C & -1/CR_{LOAD} \end{vmatrix} X + (1-D)\begin{vmatrix} 1/L \\ 0 \end{vmatrix} V_{IN} \qquad [9.0]$$

In equation [9.0] terms with the factor ***D*** arise from the first interval of the switching period, and terms with the ***(1-D)*** factor from the second interval of the switching period. The state-variable ***X*** is now the average for the entire switching period. We distribute algebraically the duty-cycle ***D*** dependence as follows:

$$Xs = D\begin{vmatrix} 0 & 0 \\ 0 & -1/CR_{LOAD} \end{vmatrix} X + D\begin{vmatrix} 1/L \\ 0 \end{vmatrix} V_{IN}$$
$$+\begin{vmatrix} 0 & -1/L \\ 1/C & -1/CR_{LOAD} \end{vmatrix} X - D\begin{vmatrix} 0 & -1/L \\ 1/C & -1/CR_{LOAD} \end{vmatrix} X + \begin{vmatrix} 1/L \\ 0 \end{vmatrix} V_{IN} - D\begin{vmatrix} 1/L \\ 0 \end{vmatrix} V_{IN} \qquad [9.1]$$

$$Xs = D\begin{vmatrix} 0 & 0 \\ 0 & -1/CR_{LOAD} \end{vmatrix} X - D\begin{vmatrix} 0 & -1/L \\ 1/C & -1/CR_{LOAD} \end{vmatrix} X$$
$$+\begin{vmatrix} 0 & -1/L \\ 1/C & -1/CR_{LOAD} \end{vmatrix} X + \begin{vmatrix} 1/L \\ 0 \end{vmatrix} V_{IN} \qquad [9.2]$$

$$Xs = \begin{vmatrix} 0 & -1/L \\ 1/C & -1/CR_{LOAD} \end{vmatrix} X - D\begin{vmatrix} 0 & -1/L \\ 1/C & 0 \end{vmatrix} X + \begin{vmatrix} 1/L \\ 0 \end{vmatrix} V_{IN} \qquad [9.3]$$

10.0 Boost Converter Initial Inductor Choice

We choose as a design requirement; a Boost Converter based on a nominal 10.2V to 14.7V $\boldsymbol{V_{IN}}$ range to supply 28V at $\boldsymbol{V_C}$ with 50 milli-Volt maximum ripple voltage. The converter must support a maximum 1 Ampere load. We constrain the minimum load to be 1% of the maximum value, or 10 milli-Amperes, using an internal load resistance. For contrasting illustrations, we choose a 2.5 MHz switching frequency.

We choose a 100 milli-Ampere peak-to-peak current ripple in the inductor as a nominal value.

From the $\boldsymbol{V_{IN}}$ range and the fixed 28V $\boldsymbol{V_C}$ value, we determine that the range of duty-cycle $\boldsymbol{D}$ must be 0.47 to 0.64. At 2.5 MHz, the times are 190 nsec to 254 nsec.

We use the 14.7V $\boldsymbol{V_{IN}}$ value during the shortest 190 nsec interval to determine the minimum inductor value that will support that voltage with the requisite current change, as follows:

$$0.1 = \Delta I_L = \frac{V_L}{L}\Delta t = \frac{14.7}{L}190 \bullet 10^{-9} \qquad [10.0]$$

$$L = \frac{14.7}{0.1} \bullet 1.9 \bullet 10^{-7} = 27.9\mu H \qquad [10.1]$$

To further address the selection of the inductor, we must consider that the Boost converter delivers a maximum of 1A at 28V or 28Watts and should not dissipate appreciable power in the inductor, while delivering that current.

The inductor must be capable of handling $\boldsymbol{I_{L\text{-}Average}}$ without saturation of the inductance, as well as have a low DC resistance. From equation [3.1], we know that $\boldsymbol{I_{Load}}$ was derived from $\boldsymbol{(1\text{-}D)\ I_{L\text{-}Average}}$ so consequently we find the maximum average inductor current as:

$$I_{L-Average} = \frac{I_{LOAD}}{1-D} = \frac{1}{1-.64} = 2.8A \qquad [10.2]$$

The power loss in the DC resistance (DCR) of the inductor is:

$$P = I^2 DCR = (2.8)^2 DCR \qquad [10.3]$$

We find a 22µH Murata component (Digikey # 811-1341-ND) that has 11mΩ □□DCR and will cause less than 1% loss at 2.8 Ampere inductor current. We consider that as acceptable.

Other considerations, including price, shielding, assembly requirements, etc., can alter other component parameters, but the inductance and DCR requirements must be met by whatever selection is made

11.0 The Simple Boost Converter Initial Capacitor Choice

We determine the minimum capacitor value from equation [5.5] as follows:

$$C_{Min} = \frac{V_C}{\Delta V_C}\frac{DT_S}{R_{Load}} = \frac{28V}{.05V} \bullet \frac{0.190 \bullet 10^{-6}\ \text{sec}}{28\Omega} = 4\mu F \qquad [11.0]$$

We can meet the first capacitor requirements with a 50V 10 µF AVX multi-layer ceramic capacitor (Digikey # 478-5048-1-ND). Again, other device parameters must be considered and these selections are for illustration only.

12.0 Switchmode Boost Power Converter Small-Signal State-Space Average Model

To model the small-signal behaviors, we introduce a notation that represents a DC operating point with "capital" letters, and small signal perturbations with the smaller letters for each variable and substitute in the model we developed in equation [9.3], as follows:

$$(X+x)s = \begin{vmatrix} 0 & -1/L \\ 1/C & -1/CR_{LOAD} \end{vmatrix}(X+x) - (D+d)\begin{vmatrix} 0 & -1/L \\ 1/C & 0 \end{vmatrix}(X+x) + \begin{vmatrix} 1/L \\ 0 \end{vmatrix}(V_{IN}+v_{IN}) \qquad [13.0]$$

We expand the terms, of equation [13.0], and remove any products of small terms as "second-order" and small enough to ignore, as follows:

$$Xs + xs = \begin{vmatrix} 0 & -1/L \\ 1/C & -1/CR_{LOAD} \end{vmatrix}X + \begin{vmatrix} 0 & -1/L \\ 1/C & -1/CR_{LOAD} \end{vmatrix}x - D\begin{vmatrix} 0 & -1/L \\ 1/C & 0 \end{vmatrix}X - d\begin{vmatrix} 0 & -1/L \\ 1/C & 0 \end{vmatrix}X - D\begin{vmatrix} 0 & -1/L \\ 1/C & 0 \end{vmatrix}x + \begin{vmatrix} 1/L \\ 0 \end{vmatrix}V_{IN} + \begin{vmatrix} 1/L \\ 0 \end{vmatrix}v_{IN} \qquad [13.1]$$

From equation [13.1], we subtract the large-signal operating-point equation given in equation [9.3], as follows:

$$xs = (Xs + xs) - Xs = \begin{vmatrix} 0 & -1/L \\ 1/C & -1/CR_{LOAD} \end{vmatrix}X + \begin{vmatrix} 0 & -1/L \\ 1/C & -1/CR_{LOAD} \end{vmatrix}x - \begin{vmatrix} 0 & -1/L \\ 1/C & -1/CR_{LOAD} \end{vmatrix}X - D\begin{vmatrix} 0 & -1/L \\ 1/C & 0 \end{vmatrix}X - d\begin{vmatrix} 0 & -1/L \\ 1/C & 0 \end{vmatrix}X - D\begin{vmatrix} 0 & -1/L \\ 1/C & 0 \end{vmatrix}x + D\begin{vmatrix} 0 & -1/L \\ 1/C & 0 \end{vmatrix}X$$

$$+\begin{vmatrix} 1/L \\ 0 \end{vmatrix} V_{IN} + \begin{vmatrix} 1/L \\ 0 \end{vmatrix} v_{IN} - \begin{vmatrix} 1/L \\ 0 \end{vmatrix} V_{IN} \qquad [13.2]$$

Collecting terms, we have the small-signal model as follows:

$$xs = \left\{ \begin{vmatrix} 0 & -\left(\frac{1}{L}\right) \\ \left(\frac{1}{C}\right) & -\left(\frac{1}{CR_{LOAD}}\right) \end{vmatrix} - D \begin{vmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & 0 \end{vmatrix} \right\} x - d \begin{vmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & 0 \end{vmatrix} X + \begin{vmatrix} \frac{1}{L} \\ 0 \end{vmatrix} v_{IN} \qquad [13.3]$$

The state-space averaged small-signal model is truly only valid for small signals. Likewise, it is only valid for small-signal perturbations with much lower frequency than the switching frequency. Serious aliasing effects can make the model unusable for frequencies approaching a large fraction of the Nyquist frequency (half the switching frequency). However, for analysis at lower frequencies to about 10% of the switching frequency, the state-space averaged model gives good results.

14.0 Small-Signal State-Space Average Model in the Frequency Domain

In classical Laplace form, we can solve the above matrix differential equation [13.3], first for the entire small-signal state variable vector ***x*** including the inductor current and then reduced to the transfer functions for the voltage output on the capacitor alone:

$$\left[sI - \left\{ \begin{vmatrix} 0 & -\left(\frac{1}{L}\right) \\ \left(\frac{1}{C}\right) & -\left(\frac{1}{CR_{LOAD}}\right) \end{vmatrix} - D \begin{vmatrix} 0 & -\left(\frac{1}{L}\right) \\ \left(\frac{1}{C}\right) & 0 \end{vmatrix} \right\} \right] x = -d \begin{vmatrix} 0 & -\left(\frac{1}{L}\right) \\ \left(\frac{1}{C}\right) & 0 \end{vmatrix} X + \begin{vmatrix} \left(\frac{1}{L}\right) \\ 0 \end{vmatrix} v_{IN} \qquad [14.0]$$

We have interpreted the large-signal quantities ***D***, and ***X*** as quasi-static constants. Only the small-signal quantities ***x***, ***d***, and $\boldsymbol{v_{IN}}$ are treated as variables. We solve by matrix inversion as follows:

$$x = \left[sI - \left\{ \begin{vmatrix} 0 & -\left(\frac{1}{L}\right) \\ \left(\frac{1}{C}\right) & -\left(\frac{1}{CR_{LOAD}}\right) \end{vmatrix} - D \begin{vmatrix} 0 & -\left(\frac{1}{L}\right) \\ \left(\frac{1}{C}\right) & 0 \end{vmatrix} \right\} \right]^{-1} \left\{ -d \begin{vmatrix} 0 & -\left(\frac{1}{L}\right) \\ \left(\frac{1}{C}\right) & 0 \end{vmatrix} X + \begin{vmatrix} \left(\frac{1}{L}\right) \\ 0 \end{vmatrix} v_{IN} \right\} \qquad [14.1]$$

In equation [14.1] above, the solution is comprised of two factors; one factor requires inversion of a 2x2 matrix and the second factor is the sum of component vectors arising from matrix algebra. We extract the matrix inversion in isolation in equation [14.2] below:

$$\left[sI - \left\{ \begin{vmatrix} 0 & -\left(\frac{1}{L}\right) \\ \left(\frac{1}{C}\right) & -\left(\frac{1}{CR_{LOAD}}\right) \end{vmatrix} - D \begin{vmatrix} 0 & -\left(\frac{1}{L}\right) \\ \left(\frac{1}{C}\right) & 0 \end{vmatrix} \right\} \right]^{-1} =$$

$$\left[s \begin{vmatrix} 1 & 0 \\ 0 & 1 \end{vmatrix} - \begin{vmatrix} 0 & -\left(\frac{1-D}{L}\right) \\ \left(\frac{1-D}{C}\right) & -\left(\frac{1}{CR_{LOAD}}\right) \end{vmatrix} \right]^{-1} = \begin{vmatrix} s & \left(\frac{1-D}{L}\right) \\ -\left(\frac{1-D}{C}\right) & \left(s+\frac{1}{CR_{LOAD}}\right) \end{vmatrix}^{-1} =$$

$$\frac{\frac{LC}{(1-D)^2}}{\frac{LC}{(1-D)^2}} \bullet \frac{1}{\left[s\left(s+\frac{1}{CR_{LOAD}}\right) + \frac{(1-D)^2}{LC} \right]} \begin{vmatrix} \left(s+\frac{1}{CR_{LOAD}}\right) & -\left(\frac{1-D}{L}\right) \\ \left(\frac{1-D}{C}\right) & s \end{vmatrix} =$$

$$\frac{1}{\left(\frac{LC}{(1-D)^2}\right)s^2 + \frac{1}{(1-D)^2}\left(\frac{L}{R_{LOAD}}\right)s + 1} \begin{vmatrix} \frac{LC}{(1-D)^2}\left(s+\frac{1}{CR_{LOAD}}\right) & -\frac{LC}{(1-D)^2}\frac{(1-D)}{L} \\ \frac{LC}{(1-D)^2}\frac{(1-D)}{C} & \frac{LC}{(1-D)^2}s \end{vmatrix} =$$

$$\frac{1}{\left(\frac{LC}{(1-D)^2}\right)s^2 + \frac{1}{(1-D)^2}\left(\frac{L}{R_{LOAD}}\right)s + 1} \begin{vmatrix} \frac{L}{(1-D)^2}\frac{1}{R_{LOAD}}(CR_{LOAD}s+1) & -\frac{C}{(1-D)} \\ \frac{L}{(1-D)} & \frac{LC}{(1-D)^2}s \end{vmatrix} \quad [14.2]$$

We define the scalar polynomial equation ***P(s)*** originating from the determinant as follows:

$$P(s) = \left(\frac{LC}{(1-D)^2}\right)s^2 + \frac{1}{(1-D)^2}\left(\frac{L}{R_{LOAD}}\right)s + 1 \quad [14.3]$$

As we examine the polynomial, we are reminded that during the $\boldsymbol{DT_S}$ interval, the inductor and capacitor are effectively disconnected. Conversely, if the duty-cycle is reduced to zero,

the inductor and capacitor are effectively always connected. In the event that ***D = 0***, then we express ***P(s)*** as:

$$P(s)\big|_{D=0} = LCs^2 + \left(\frac{L}{R_{LOAD}}\right)s + 1 \qquad [14.4]$$

We note that equation [14.4] correctly describes poles of second-order LC resonant circuit connecting the input to the output.

For the matrix inversion, we conclude with:

$$\left[sI - \begin{vmatrix} 0 & -\left(\frac{1}{L}\right) \\ \left(\frac{1}{C}\right) & -\left(\frac{1}{CR_{LOAD}}\right) \end{vmatrix} - D \begin{vmatrix} 0 & -\left(\frac{1}{L}\right) \\ \left(\frac{1}{C}\right) & 0 \end{vmatrix} \right]^{-1} =$$

$$\frac{1}{P(s)}\frac{1}{(1-D)} \begin{vmatrix} \frac{1}{(1-D)}\frac{L}{R_{LOAD}}(CR_{LOAD}s+1) & -C \\ L & \frac{LC}{(1-D)}s \end{vmatrix} \qquad [14.5]$$

We move the scalar polynomial equation ***P(s)*** and ***(1-D)*** factor to become a multiplying factor for the small-signal state vector ***x*** in the differential equation solution for the entire model and equation [14.1] becomes equation [14.6] below as follows:

$$(1-D)P(s)x = \begin{vmatrix} \frac{1}{(1-D)}\frac{L}{R_{LOAD}}(CR_{LOAD}s+1) & -C \\ L & \frac{LC}{(1-D)}s \end{vmatrix} \left\{ -d \begin{vmatrix} 0 & -\left(\frac{1}{L}\right) \\ \left(\frac{1}{C}\right) & 0 \end{vmatrix} X + \begin{vmatrix} \left(\frac{1}{L}\right) \\ 0 \end{vmatrix} v_{IN} \right\} \quad [14.6]$$

In equation [14.6] above, the ***P(s)*** polynomial equation in the LaPlace operator "***s***" is a scalar quantity and multiplies the small-signal state vector ***x***, but there is a 2x2 matrix from the matrix inversion to be distributed across a 2x2 ***d*** dependency matrix and a 2x1 $\boldsymbol{v_{IN}}$ dependency vector to simplify the model.

In equation [14.7] below, we perform the distributive 2x2 matrix multiplication in isolation as part of the solution as follows:

$$-d\begin{vmatrix} \frac{1}{(1-D)}\frac{L}{R_{LOAD}}(CR_{LOAD}s+1) & -C \\ L & \frac{LC}{(1-D)}s \end{vmatrix}\bullet\begin{vmatrix} 0 & -\left(\frac{1}{L}\right) \\ \left(\frac{1}{C}\right) & 0 \end{vmatrix}X =$$

$$-d\begin{vmatrix} -1 & -\frac{1}{(1-D)}\frac{1}{R_{LOAD}}(CR_{LOAD}s+1) \\ \frac{Ls}{(1-D)} & -1 \end{vmatrix}X \qquad [14.7]$$

We use the partial result from equation [14.7] above to substitute in equation [14.6] to form equation [14.8] below as follows:

$$(1-D)P(s)x = -d\begin{vmatrix} -1 & -\frac{1}{(1-D)}\frac{1}{R_{LOAD}}(CR_{LOAD}s+1) \\ \frac{Ls}{(1-D)} & -1 \end{vmatrix}X + \begin{vmatrix} \frac{1}{(1-D)}\frac{1}{R_{LOAD}}(R_{LOAD}Cs+1) \\ 1 \end{vmatrix}v_{IN} \qquad [14.8]$$

We restate explicit small-signal equations individually, as follows:

$$(1-D)P(s)i_L = dI_L + d\frac{1}{(1-D)}\frac{1}{R_{LOAD}}(R_{LOAD}Cs+1)V_C + \frac{1}{(1-D)}\frac{1}{R_{LOAD}}(R_{LOAD}Cs+1)v_{IN} \qquad [14.9]$$

$$(1-D)P(s)v_C = -d\frac{L}{(1-D)}sI_L + dV_C + v_{IN} \qquad [14.10]$$

15.0 Feedforward Control Option for Good Line Regulation

We see that equation [14.9] indicates that the output voltage across the capacitor has a small-signal dependency on both the input voltage $\boldsymbol{v_{IN}}$ and the duty cycle $\boldsymbol{d}$ so that we can find the conditions that reduce the sum to be zero, as follows:

$$(1-D)P(s)v_C = 0 = -d_{ff}\frac{L}{(1-D)}sI_L + d_{ff}V_C + v_{IN} = 0 \qquad [15.0]$$

We solve equation [15.0], using d_{ff} to represent the feed-forward component of the duty-cycle variation as follows:

$$d_{ff}\frac{L}{(1-D)}sI_L - d_{ff}V_C = v_{IN} \qquad [15.1]$$

$$d_{ff}V_C\left(\frac{1}{(1-D)}\frac{L}{V_C/I_L}s-1\right) = v_{IN} \qquad [15.2]$$

$$d_{ff} = \frac{1}{\left(\frac{1}{(1-D)}\frac{L}{V_C/I_L}s-1\right)}\frac{v_{IN}}{V_C} \qquad [15.3]$$

From equation [15.3], we found a single-pole relationship that is required to eliminate the small-signal supply perturbation effects on the output voltage. We defer any implementation discussion but note that we would require a duty-cycle control signal with right-half-plane characteristics defined in equation [15.3] to provide optimum feed-forward line regulation.

16.0 Feedback Control Option for Good Load Regulation

From equation [14.10] we isolate the small-signal dependency of the v_C capacitor voltage on the duty-cycle. We retain only the dependency of the capacitor voltage v_C on the feedback duty cycle d_{fb} as follows:

$$(1-D)P(s)v_C = -d_{fb}\frac{L}{(1-D)}sI_L + d_{fb}V_C \qquad [16.0]$$

$$(1-D)P(s)v_C = -d_{fb}\left(\frac{1}{(1-D)}\frac{L}{V_C/I_L}s-1\right)V_C \qquad [16.1]$$

$$v_C = -d_{fb}\frac{1}{(1-D)}\frac{\left(\frac{1}{(1-D)}\frac{L}{V_C/I_L}\right)s-1}{P(s)}V_C \qquad [16.2]$$

$$Boost(s) = \frac{v_C}{d_{fb}} = -\frac{V_C}{(1-D)}\left[\frac{\left(\frac{1}{(1-D)}\frac{L}{V_C/I_L}\right)s-1}{\left(\frac{LC}{(1-D)^2}\right)s^2+\left(\frac{1}{(1-D)^2}\frac{L}{R_{LOAD}}\right)s+1}\right] \qquad [16.3]$$

The objective of feedback control is to maintain the value of $\boldsymbol{V_C}$, so we can treat that quantity as quasi-static. Because the output capacitor is not involved in any DC currents, we can express the Load current through $\boldsymbol{R_{Load}}$ as the average of the duty-cycle modulated inductor current or $(\boldsymbol{1\text{-}D})\boldsymbol{I_L}$ and from Ohm's Law:

$$V_C = (1-D)I_L R_{Load} \qquad [16.4]$$

$$I_L = \frac{1}{(1-D)}\frac{V_C}{R_{Load}} \qquad [16.5]$$

$$Boost(s) = -\frac{V_C}{(1-D)}\left[\frac{\left(\frac{1}{(1-D)}\frac{L}{V_C\Big/\frac{1}{(1-D)}\frac{V_C}{R_{Load}}}\right)s-1}{\left(\frac{LC}{(1-D)^2}\right)s^2+\left(\frac{1}{(1-D)^2}\frac{L}{R_{LOAD}}\right)s+1}\right] \qquad [16.6]$$

$$Boost(s) = -\frac{V_C}{(1-D)}\left[\frac{\left(\frac{1}{(1-D)^2}\frac{L}{R_{Load}}\right)s-1}{\left(\frac{LC}{(1-D)^2}\right)s^2+\left(\frac{1}{(1-D)^2}\frac{L}{R_{LOAD}}\right)s+1}\right] \qquad [16.7]$$

Equation [16.7] expresses the small-signal dependency of the output voltage on the duty-cycle. We defer discussion of how the duty-cycle variation is developed from the feedback.

We construct a typical block diagram for the development of open and closed-loop behaviors as follows:

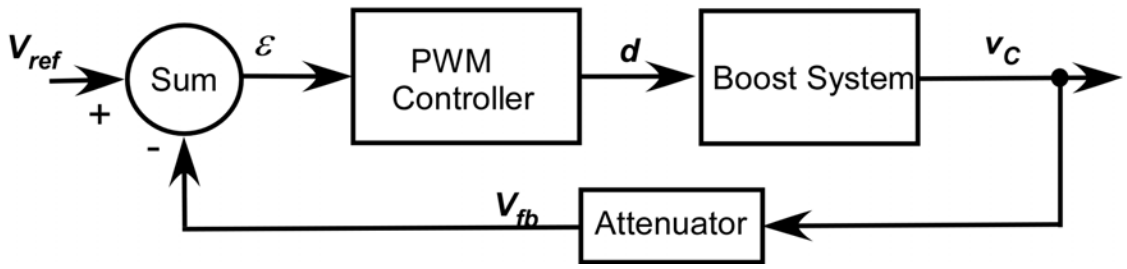

Figure 16.0 Boost Converter Small-Signal Voltage-Mode Controller Block Diagram

The PWM Controller converts the error voltage $\boldsymbol{\varepsilon}$ into the clocking signal with the duty-cycle $\boldsymbol{d}$ for control of the Boost switching. In that respect, $\boldsymbol{\varepsilon}$ is a small-signal quantity itself. The $\boldsymbol{V_{ref}}$ signal is typically a DC value developed from a "Bandgap" or some form of Voltage reference but not necessarily at the same level as the desired output $\boldsymbol{V_C}$ voltage. The "Attenuator" reduces the $\boldsymbol{V_C}$ voltage value so that it can be compared to the $\boldsymbol{V_{ref}}$ value and thus produces the $\boldsymbol{\varepsilon}$ error signal.

We model both the PWM Controller $\boldsymbol{T_{PWM}}$ and the Attenuator $\boldsymbol{T_{ATTEN}}$ as wide-bandwidth transfer functions to produce an open-loop transfer function:

$$T(s) = T_{PWM}(s)T_{ATTEN}\,Boost(s) \qquad [16.8]$$

In standard form:

$$T(s) = -T_{PWM}(s)T_{ATTEN}\frac{V_C}{(1-D)}\left[\frac{\frac{1}{\omega_Z}s-1}{\frac{1}{\omega_0^2}s^2+\frac{2\zeta}{\omega_0}s+1}\right] =$$

$$-T_{PWM}(s)T_{ATTEN}A_{Boost}\left[\frac{\frac{1}{\omega_Z}s-1}{\frac{1}{\omega_0^2}s^2+\frac{2\zeta}{\omega_0}s+1}\right] \qquad [16.9]$$

Thus far, our open-loop frequency dependencies lie in the operating point variables $\boldsymbol{D}$ and $\boldsymbol{V_C}$, and the second-order combination of the LC components, but the damping factor $\boldsymbol{\zeta}$ also depends on the equivalent value of $\boldsymbol{R_{LOAD}}$ on damping the transfer function. From the standard form of the denominator, we have:

$$A_{Boost} = -\frac{V_C}{(1-D)} \qquad [16.10]$$

$$\omega_Z = \frac{1}{\left(\frac{1}{(1-D)^2}\frac{L}{R_{LOAD}}\right)} = (1-D)^2\frac{R_{LOAD}}{L} \qquad [16.11]$$

From equation [16.9] we know that the zero lies in the right-half plane and cannot be cancelled by what would be an unstable pole in the PWM controller. From equation [16.11], we know that the location of the zero depends on the $\boldsymbol{R_{Load}}$ resistance as well as the ***D*** duty-cycle.

$$\omega_0 = \frac{1}{\sqrt{\frac{LC}{(1-D)^2}}} = \frac{1-D}{\sqrt{LC}} \qquad [16.12]$$

$$\frac{2\varsigma}{\omega_0} = \frac{1}{(1-D)^2}\frac{L}{R_{LOAD}} = \frac{1}{\omega_z} \qquad [16.13]$$

$$\varsigma = \frac{\omega_0}{2\omega_z} = \frac{\frac{1-D}{\sqrt{LC}} \bullet L}{2(1-D)^2 R_{LOAD}} = \frac{1}{2(1-D)}\frac{1}{R_{LOAD}}\sqrt{\frac{L}{C}} \qquad [16.14]$$

Boost P-Z Summary

				Rload = 28			Rload = 280		
D	**A_{Boost}**	**ω_0**	**f_0**	**ω_z**	**f_z**	**ζ**	**ω_z**	**f_z**	**ζ**
0	28	67.4k rad/s	10.7kHz	1.27M rad/s	203kHz	0.0265	12.7M rad/s	2.03MHz	0.00265
0.7	93.3	20.2k rad/s	3.22kHz	115k rad/s	18.2kHz	0.0883	1.15M rad/s	182kHz	0.00883

Table 16.0 Boost Small-Signal Transfer Function Pole and Zero Behavior

17.0 Boost Small-Signal Transfer Function Bode Plot Variations

The second-order Pole locus depends on the LC component choices made earlier to address the ripple concerns, but also depend on the operating point duty-cycle ***D*** from the turn-on instant up to the nominal worst-case operating point. In addition, both the resonant peaking as well as a right-half plane zero depend also on the equivalent $\boldsymbol{R_{Load}}$ load resistor.

We do not explicitly control the selection of the duty-cycle D, but rather accept it as imposed by the required operating point and as a result of the control function. Likewise, we do not explicitly control the selection of the $\boldsymbol{R_{Load}}$ load resistor, rather it is the result of the DC load requirements placed on the converter. Both are "exogeneous" or external quantities that we

must provide a compensation scheme for Boost converter pole-zero variations in the design of the controller.

We show Bode plots of our small-signal model as we vary the exogenous duty-cycle **D** and R_{Load} load resistor variables over their expected range of operation.

Figure 17.0 below shows the expected variations in DC gain (increases with larger ***D***), as well as the decrease in resonant frequency (decreases with larger ***D***), but also shows the effect of the varying right-half plane ω_z zero adding 90° to the asymptotic phase at frequencies above the ω_0 resonance.

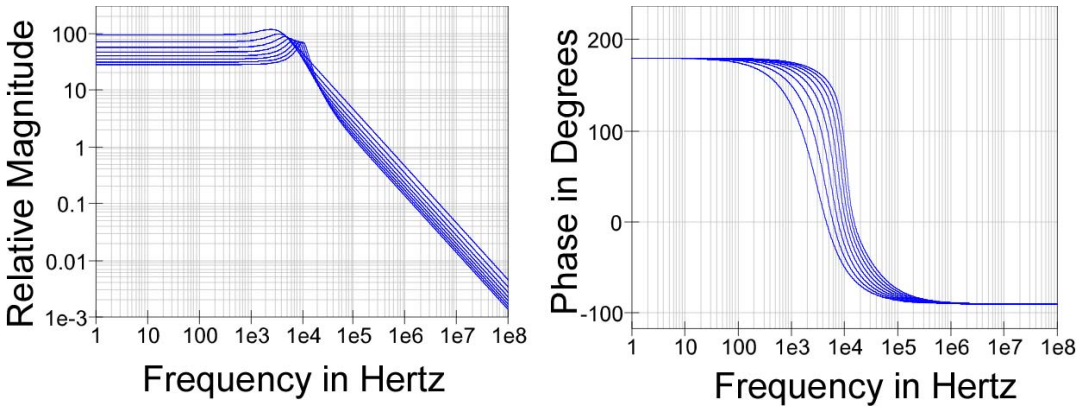

Figure 17.0 Boost Small-Signal Transfer Function Bode Plot: 0 < D <0.7, 1 Amp Load

Because figure 17.0 above shows simulations with the greatest load current corresponding to R_{Load} = 28 Ω, it also presents the greatest damping and the resonant peaking is relatively small. It is also difficult to discern the magnitude effects of the right-half plane ω_z zero. We would expect to encounter such a situation whenever there are wide variations in the V_{IN} value, but R_{Load} is constant.

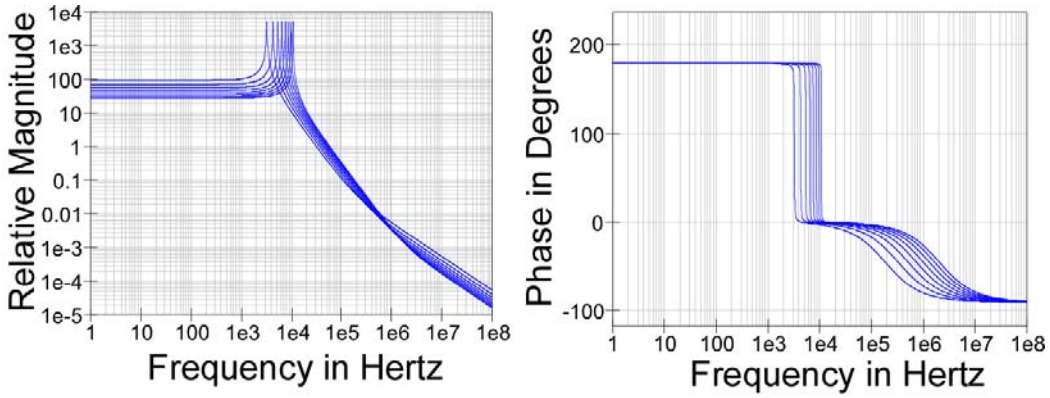

Figure 17.1 Boost Small-Signal Transfer Function Bode Plot: 0 < D <0.7, 0.1 Amp Load

Simulations in figure 17.1 are similar to those of figure 17.0, but under a minimum load condition corresponding to the R_{Load} = 280 Ω value. Figure 17.1 shows the expected variations in DC gain, as well as the decrease in ω_0 resonant frequency. The peaking and rapid phase changes at resonance are more pronounced and present control challenges. It is less difficult to discern the magnitude and phase effects of the right-half plane ω_z zero. Again, we would expect to encounter such a situation whenever there are wide variations in the V_{IN} value, but R_{Load} is light, but constant.

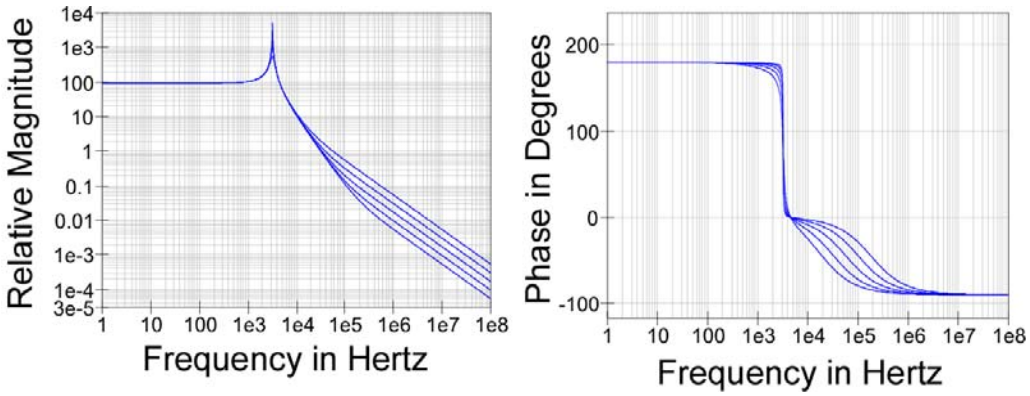

Figure 17.2 Boost Small-Signal Bode Plot: D => 0, 0.1 to 1 Amp Load

Figure 17.2 simulations above are performed with constant D = 0 and results in no variation in DC gain or the ω_0 resonant frequency, but shows the R_{Load} variations cause ζ variations in resonant peaking and phase slope around the ω_0 resonant frequency, and the frequency variations of the magnitude and phase of the right-half plane ω_z zero above the ω_0 resonance also change. We expect to encounter this situation with D = 0 whenever V_{IN} nearly equals the target V_C value and both are constant, but R_{Load} is changing.

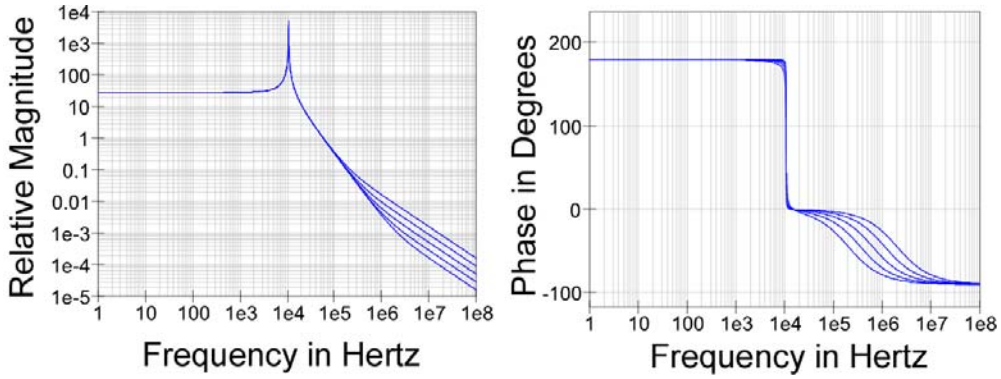

Figure 17.3 Boost Small-Signal Bode Plot: D => 0.7, 0.1 Amp Load

Figure 17.3 simulations above are similar to those of figure 17.2 but are performed with constant $\boldsymbol{D}$ = 7 corresponding to the greatest expected difference between $\boldsymbol{V_{IN}}$ and the target $\boldsymbol{V_C}$ value. Again, we encounter no variation in DC gain or the $\boldsymbol{\omega_0}$ resonant frequency, but shows the $\boldsymbol{R_{Load}}$ variations cause $\boldsymbol{\zeta}$ variations in resonant peaking and phase slope around the $\boldsymbol{\omega_0}$ resonant frequency, as well as frequency variations of the magnitude and phase of the right-half plane $\boldsymbol{\omega_z}$ zero above the $\boldsymbol{\omega_0}$ resonance.

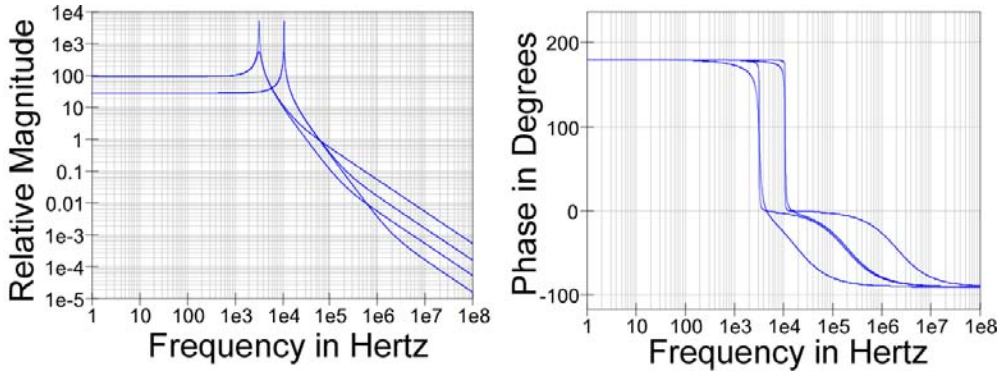

Figure 17.4 Boost Small-Signal Bode Plot: D =0, 0.7; Load = 0.1, 1 Amp

Figure 17.4 shows the extreme values for the expected variations in DC gain, resonant frequencies, peaking, the range of phase slope through the resonant frequencies, and the frequency variations of the magnitude and phase associated with the right-half plane zero above the resonance. The PWM controller must function over this entire range of behaviors.

18.0 Discrete-Time effects of a Pulse-Width Modulator (PWM)

A Pulse Width Modulator (PWM) block adds a discrete-time sampling effect with an equivalent $T_{ZOH}(s)$ "Zero-Order-Hold" (ZOH) transfer function within the loop. State-space averaging prevents us from having an average value for a cycle of the PWM until the cycle is complete. To model the PWM, we utilize the well-known ZOH behavior inside the loop, with an average half-cycle delay at the sampling rate, applied to each sample.

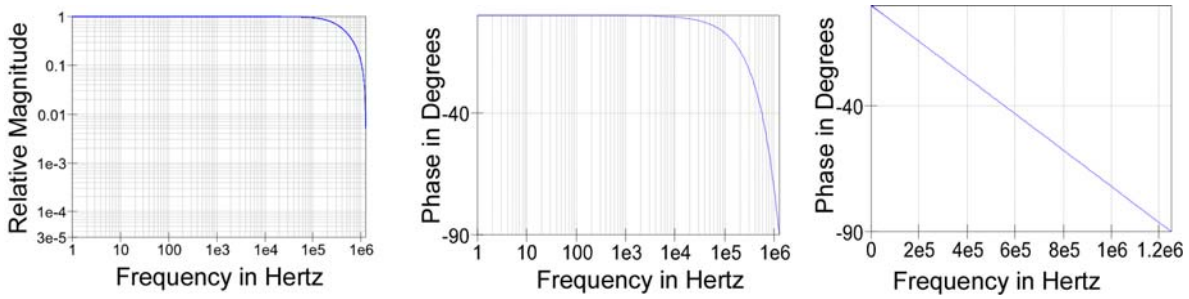

Figure 18.0 Zero-Order Hold Magnitude and Phase

A consequence introduced by the ZOH is the magnitude "notch" introduced by the ZOH at the Nyquist frequency. No magnitude information is available at the Nyquist rate. The magnitude envelope is the shape of a "cosine" with the argument equal to the ratio:

$$|ZOH| = \cos\left(2\pi \frac{f}{f_s}\right) \qquad [18.0]$$

The ZOH delay behavior also adds additional phase delay in the phase response for the loop caused by the full-cycle sampling delay. The average delay is one-half-cycle (180^o) at the sampling frequency implies half that value (90^o) at the Nyquist frequency. In figure 18.0, we show the linear phase to the right on a linear frequency scale. The $d\phi/d\omega$ is identically the constant delay. For convenience, the phase is also shown on a logarithmic frequency scale in the center of the illustration so that phase and magnitudes (from the left illustration), can more easily be associated.

19.0 Pole-Zero Compensation for the 2.5 MHz Boost Converter Loop

We have seen that the particular example is composed of an LC behavior with modifications for a Nyquist "notch" and delay, both related to the sampling inherent in the switching/averaging nature of the conversion. These effects notwithstanding, the network is still dominated by duty-cycle D and R_{Load} variations of the Boost small-signal behaviors.

$$T(s) = -T_{PWM}(s)T_{ATTEN}A_{Boost}\left[\frac{\frac{1}{\omega_Z}s - 1}{\frac{1}{\omega_0^2}s^2 + \frac{2\varsigma}{\omega_0}s + 1}\right] \qquad [19.0]$$

We introduce a Pole-Zero (PZ) compensation scheme as well as the ZOH model, within the PWM as follows:

$$T_{PWM}(s) = T_{ZOH}(s) \bullet T_{PZ}(s) = T_{ZOH}(s) \bullet \frac{\left(\frac{1}{\omega_Z^2}s^2 + \frac{2\varsigma_Z}{\omega_Z}s + 1\right)}{\left(\frac{1}{\omega_{P1}}s + 1\right)\left(\frac{1}{\omega_{P2}}s + 1\right)\left(\frac{s}{\omega_{Int}}\right)} \qquad [19.1]$$

The purpose of the PZ compensator is to introduce an integrator at ω_{Int} to increase the DC loop gain at low frequencies to reduce DC error, and effectively introduce phase shifts to reduce the total phase introduced by the Boost behavior at lower frequencies as follows

$$T(s) = -T_{ATTEN}T_{ZOH}(s)A_{Boost}\left[\frac{\left(\frac{1}{\omega_{Comp-z}^2}s^2 + \frac{2\varsigma_{Zero}}{\omega_{Comp-z}}s + 1\right)}{\left(\frac{1}{\omega_{Pole}^2}s^2 + \frac{2\varsigma_{Pole}}{\omega_{Pole}}s + 1\right)\left(\frac{s}{\omega_{Int}}\right)}\right]\left[\frac{\frac{1}{\omega_Z}s - 1}{\frac{1}{\omega_0^2}s^2 + \frac{2\varsigma}{\omega_0}s + 1}\right] \qquad [19.2]$$

We design the PZ compensator with a complex-conjugate $\omega_{Comp\text{-}Z}$ zero pair with locations 10% below the lowest expected ω_0 resonance frequency. We place the PZ double ω_{Pole} real poles obtained by making $\zeta_{Pole} = 1$, at a higher frequency and depend on the remaining ω_{Int} integrator magnitude slope to bring the gain to unity.

The relatively small DC gain of the Boost function prompts the addition of the substantial DC gain of the integrator to reap the rewards of the feedback control for error reduction. But, simply adding the integrator gain also increases the unity-gain frequency of the open loop and, with that increase in unity-gain frequency, we could also lose phase margin.

$$|T_{PZ}(j\varpi)| = \frac{\sqrt{\left(1 - \left(\frac{\omega}{\omega_{Comp-Z}}\right)^2\right)^2 + \left(2\frac{\omega}{\omega_{Comp-Z}}\varsigma_{Zero}\right)^2}}{\left(\frac{\omega}{\omega_{Int}}\right)\left(1 + \left(\frac{\omega}{\omega_{Pole}}\right)^2\right)} \qquad [19.3]$$

$$\theta_{PZ}(j\varpi) = -90^{o} + \tan^{-1}\left(\frac{2\dfrac{\omega}{\omega_{Comp-Z}}\varsigma_{Zero}}{1-\left(\dfrac{\omega}{\omega_{Comp-z}}\right)^{2}}\right) - 2\tan^{-1}\left(\frac{\omega}{\omega_{Pole}}\right) \qquad [19.4]$$

We choose to place the two pole frequencies far above the zeroes. The intention is to use the phase "lead" of the zero pair to compensate for the two-pole "lag" of the varying ω_0 resonance and defer replacing the ω_{Pole} two pole "lag" until above the unity-gain frequency. We employ a state-variable filter shown in schematic form in figure 19.0 below to realize the appropriate PZ compensation. The active filter realization is useful for obtaining the complex-conjugate ω_{Comp-Z} zero locations and relatively large phase slopes that are available as a consequence. The ω_{Pole} real pole-pair location is easily realized by the topology and relatively inexpensive amplifiers can be employed.

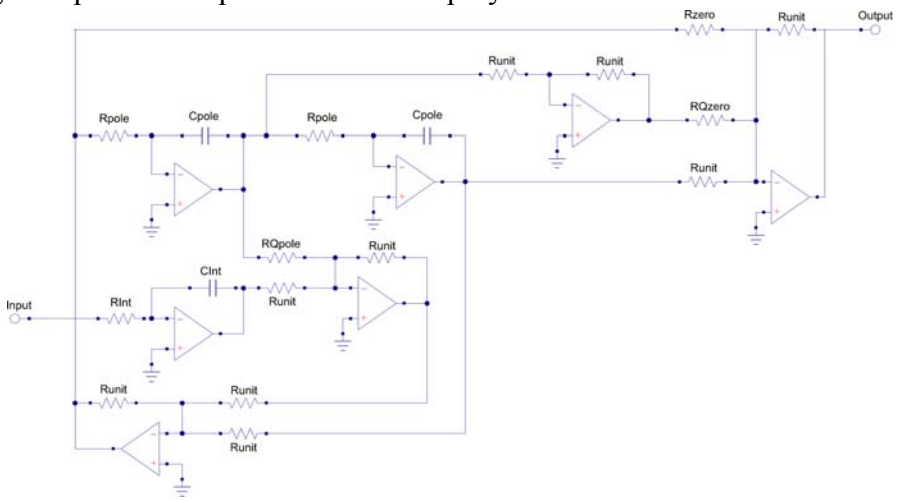

Figure 19.0 State-Variable Filter Schematic for PZ Compensation

The State-Variable filter shown in figure 19.0 above can easily be "tuned" using the following design equations:

$$\tau_{Int} = R_{Int}C_{Int} = 0.002\,\text{sec} \qquad [19.5]$$

$$f_{Int} = \frac{1}{2\pi\tau_{Int}} = 800Hz \qquad [19.6]$$

$$\tau_{Pole} = R_{Pole}C_{Pole} = 2\mu\,\text{sec} \qquad [19.7]$$

$$f_{Pole} = \frac{1}{2\pi\tau_{Pole}} = 80kHz \qquad [19.8]$$

$$R_{Q-Pole} = \frac{R_{Unit}}{2} \qquad [19.9]$$

$$R_{Zero} = \left(\frac{f_{Zero}}{f_{Pole}}\right)^2 R_{Unit} \qquad [19.10]$$

$$f_{Zero} = f_{Pole}\sqrt{\frac{R_{Zero}}{R_{Unit}}} = f_{Pole}\sqrt{.001} = 2.5kHz \qquad [19.11]$$

$$R_{Q-Zero} = \frac{1}{2\varsigma_{Zero}}\left(\frac{f_{Zero}}{f_{Pole}}\right)R_{Unit} \qquad [19.12]$$

$$\varsigma_{Zero} = \frac{1}{2}\left(\frac{f_{Zero}}{f_{Pole}}\right)\left(\frac{R_{Unit}}{R_{Zero}}\right) = 10\sqrt{.001} = .32 \qquad [19.13]$$

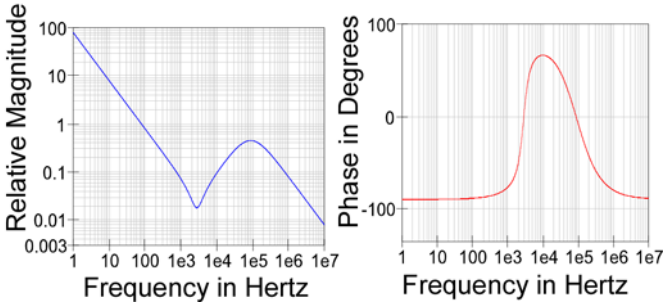

Figure 19.1 State-Variable Filter PZ Compensation Bode Plots

20.0 Open Loop Behavior for the 2.5 MHz Boost Converter

We show sets of three Bode plots for the Boost converter: first, in isolation, second, for the Boost converter with the PZ compensation included, and third, with the ZOH effects included. The sets of three plots are presented starting with the startup conditions at $\boldsymbol{D = 0}$ and $\boldsymbol{R_{Load}} = 280\Omega$ light load, followed by $\boldsymbol{R_{Load}} = 28\Omega$ maximum load, then under the nominal operating conditions with $\boldsymbol{D = 0.7}$ and $\boldsymbol{R_{Load}} = 280\Omega$ light load, followed by $\boldsymbol{R_{Load}} = 28\Omega$ maximum load.

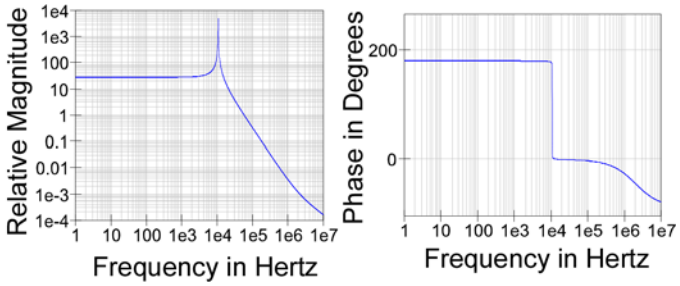

Figure 20.0a Boost Converter Bode Plot: D = 0, 280 Ω Load

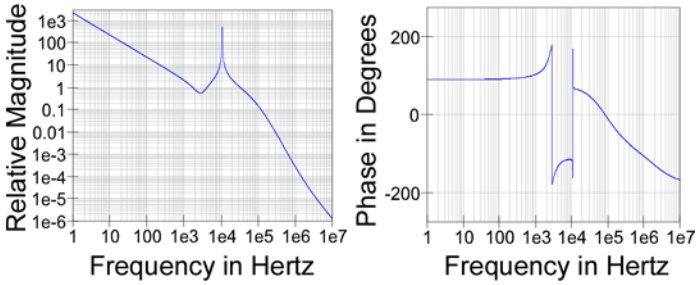

Figure 20.0b Boost with PZ Compensation Bode Plot: D = 0, 280 Ω Load

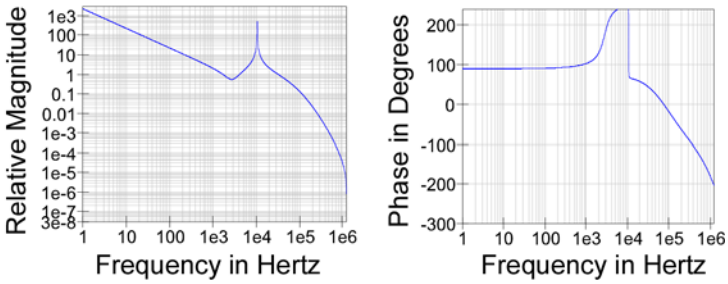

Figure 20.0c Boost with PZ & ZOH Compensation Bode Plot: D = 0, 280 Ω Load

Figure 20.0c shows that the open loop gain crosses unity several times during these conditions, but the phase margin is greater than 50^{o} in all cases. We have included the case with ***D* = 0** to ensure stability at startup, but the conditions are expected to be transitory.

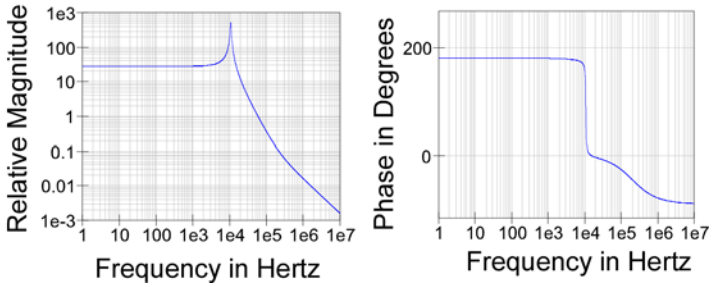

Figure 20.1a Boost Converter Bode Plot: D = 0, 28 Ω Load

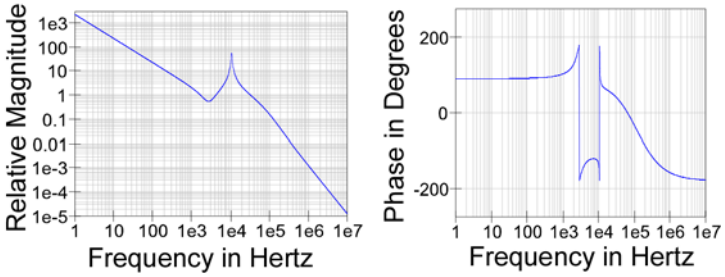

Figure 20.1b Boost with PZ Compensation Bode Plot: D = 0, 28 Ω Load

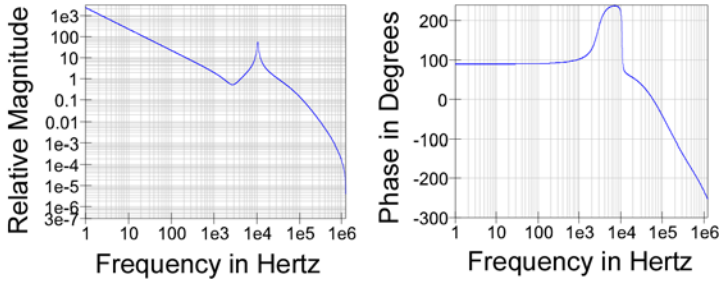

Figure 20.1c Boost with PZ & ZOH Compensation Bode Plot: D = 0, 28 Ω Load

Figure 20.1c above shows that the open loop gain again crosses unity several times during these conditions, but the phase margin is greater than 50^{o} in all cases. We have included the case with ***D* = 0** to ensure stability at startup under maximum load, but these conditions are expected to be transitory, too.

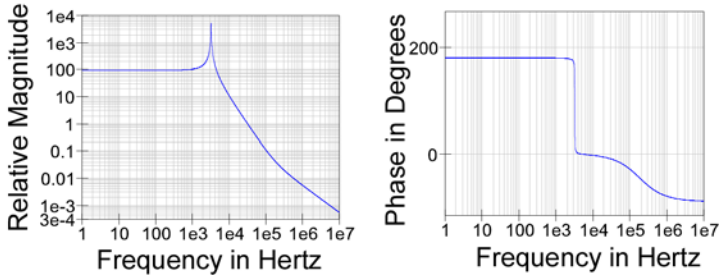

Figure 20.2a Boost Converter Bode Plot: D = 0.7, 280 Ω Load

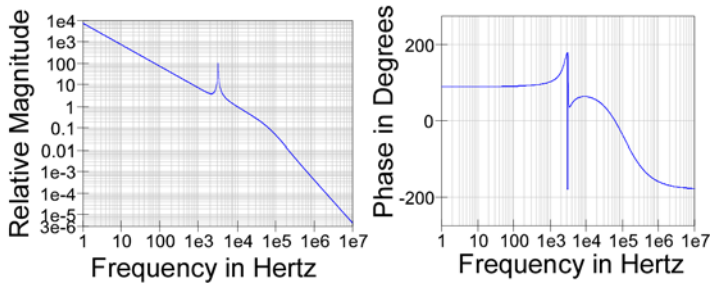

Figure 20.2b Boost with PZ Compensation Bode Plot: D = 0.7, 280 Ω Load

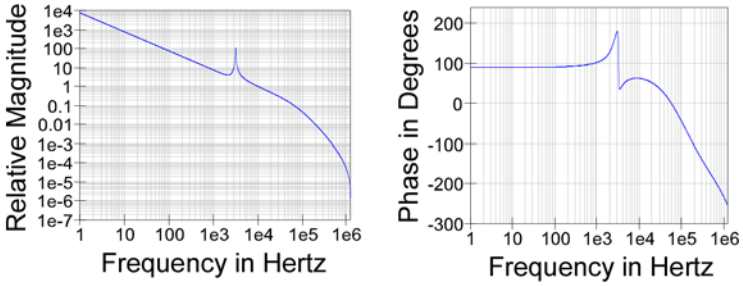

Figure 20.2c Boost with PZ & ZOH Compensation Bode Plot: D = 0.7, 280 Ω Load

Figure 20.2c above shows that the open loop gain again crosses unity at ~10kHz under these conditions, but the phase margin is greater than 50^{o} up to that frequency.

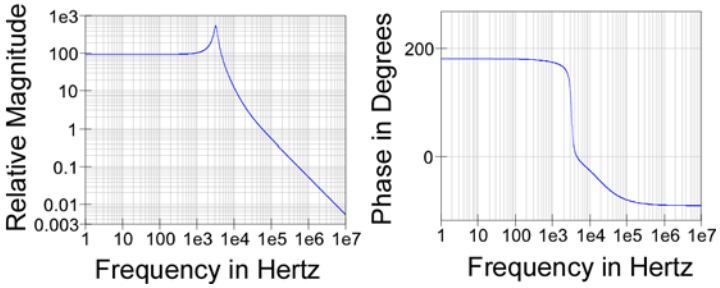

Figure 20.3a Boost Converter Bode Plot: D = 0.7, 28 Ω Load

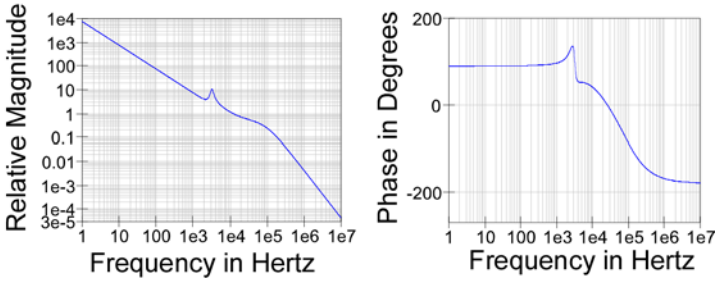

Figure 20.3b Boost with PZ Compensation Bode Plot: D = 0.7, 28 Ω Load

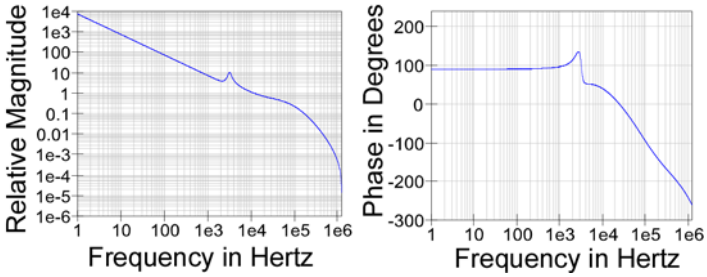

Figure 20.3c Boost with PZ & ZOH Compensation Bode Plot: D = 0.7, 28 Ω Load

Figure 20.3c above shows that the open loop gain again crosses unity at ~10kHz under these conditions, but the phase margin is greater than 50^{o} up to that frequency.

21.0 Pulse-Width Modulator

It is common practice to use a triangular waveform and a comparator to provide the Pulse-Width Modulation (PWM) function shown in figure 16.0. Various triangular wave shapes have been used from sawtooth to symmetrical triangles, but all translate a voltage at the comparator input into a duty-cycle. We develop the following waveforms:

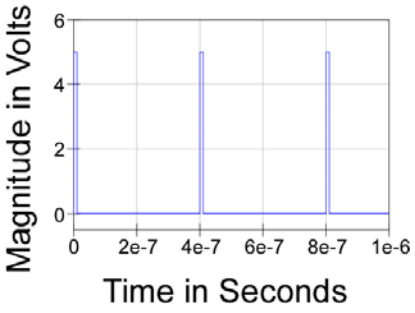

Figure 21.0 Pulse Oscillator at 2.5MHz

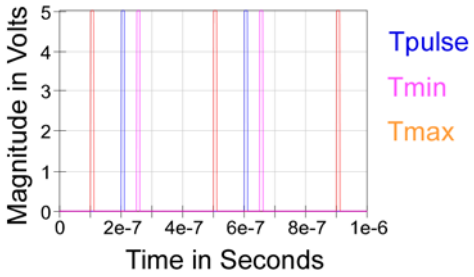

Figure 21.1 The Pulse Oscillator with Two Delayed Replicas

We produce a pulse oscillator timing references shown in figure 21.0 as a short duration pulse train with the period equal to the T_S sampling period. In this example, the 2.5Mhz pulse oscillator has a T_S period of 400 nanoseconds and a duration of ~10 nanoseconds.

The two delayed versions shown in figure 21.1, one designated with a T_{min} delay, and the second with a longer T_{max} delay relative to the T_{pulse} pulse oscillator reference waveform improve timing accuracy for control purposes. Implementations that control timing of these delays is possible with less than 10% uncertainty of each delay.

We define the delay between the pulse oscillator and the pulse designated as the shorter delay as $T_{on\text{-}Min}$ for reasons that will also become apparent.

We employ a Flip/Flop as a Pulse-Width Modulator (PWM). We initiate all PWM periods with the T_{pulse} waveform. In each PWM period the initiation by the T_{pulse} waveform is called T_{Start}. The period of the PWM is controlled so that it terminates on one of three events, the waveform designated as the T_{min} waveform, the next T_{max} waveform, or a pulse that occurs between the two. The $T_{on\text{-}Min}$ duration is ~50 nanoseconds for a minimum D duty-cycle of 50/400 = ~12.5% but the $T_{off\text{-}Min} = T_S - T_{max}$ duration is ~100 nanoseconds for a maximum D duty-cycle of (400-100)/400 = ~75%.

To initialize the PWM Flip/Flop, we employ a reset pulse shown in figure 16.2 that is derived from start-up logic designating that a logic high means the implementation is not ready and conversely the logic low enables the PWM Flip/Flop.

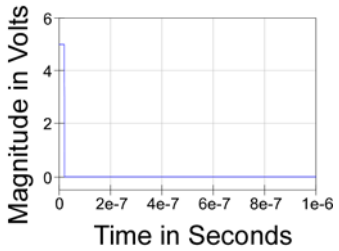

Figure 21.2 The Supervisory "Reset" Signal to Permit Timing to Commence

The pulse oscillator periodically resets a ramp generator and produces typical sawtooth waveforms as follows:

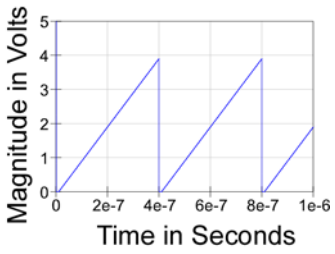

Figure 21.3 Sawtooth Oscillator at 2.5MHz

We obtain the ramp from a current source charging a capacitor and periodically discharge the capacitor to zero volts under control of the PWM.

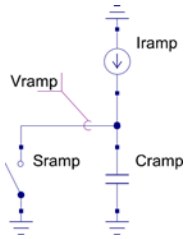

Figure 21.4 Simple Sawtooth Oscillator Schematic

The slope is given by:

$$Slope = \frac{dV_{ramp}}{dt} = \frac{I_{ramp}}{C_{ramp}} \qquad [21.1]$$

For the $\boldsymbol{I_{ramp}}$ current of 1milli-Ampere and a $\boldsymbol{C_{ramp}}$ value of 100 pF, the ***Slope*** is:

$$Slope = \frac{dV_{ramp}}{dt} = \frac{I_{ramp}}{C_{ramp}} = \frac{1 \bullet 10^{-3}}{1 \bullet 10^{-10}} = 10 \frac{V}{\mu \sec} \qquad [21.2]$$

In 400 nsec $\boldsymbol{T_S}$, we attain a 4V signal magnitude and the pulse oscillator resets the capacitor voltage to zero, starting a new cycle at 2.5 MHz.

Using the same charging/discharging circuitry, we can scale the behavior of the sawtooth waveform by choosing different capacitor values.

Similarly, we can also scale the ramp rate ***Slope*** by controlling the charging current. Increasing the current increases the ramp rate, while decreasing the current decreases the ***Slope***.

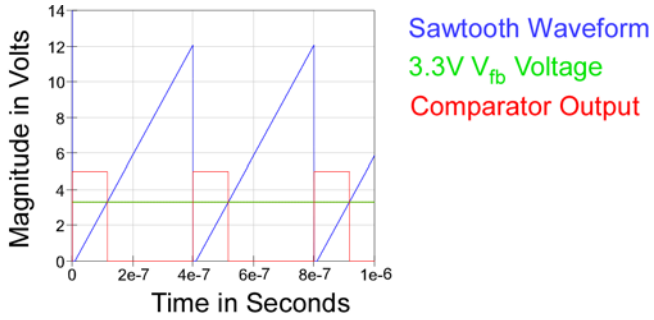

Figure 21.3 Pulse Width Modulation (PWM) Discussion Waveforms

We have taken liberties with the magnitudes in figure 21.3 to enable clarity in the discussions that follow. We have retained the 2.5M Hz T_S timing of a 400 nsec cycle, but scaled the sawtooth peak magnitude to 12V to enable discussions of "similar triangles" in the following discussion. For the example illustrated in figure 21.3, the slope is:

$$Slope = \frac{dV_{ramp}}{dt} = \frac{12V}{400n\,\text{sec}} = 30\frac{V}{\mu\,\text{sec}} \qquad [21.4]$$

And, indirectly, the V_{Peak} peak voltage in this case is:

$$V_{Peak} = \frac{dV_{ramp}}{dt} \bullet T_S = 30\frac{V}{\mu\,\text{sec}} \bullet 0.4\mu\,\text{sec} = 12V \qquad [21.5]$$

At the prescribed 30V/µsec slope, we require 110 nsec to reach the 3.3V switching point of the comparator set by the 3.3V V_{fb} feedback voltage. It takes the full 400 nsec to reach the 12V V_{Peak} peak value. The comparator output waveform duty cycle is:

$$D = \frac{T_{ON}}{T_S} = \frac{110n\,\text{sec}}{400n\,\text{sec}} = 0.275 = \frac{V_{fb}}{V_{Peak}} = \frac{3.3V}{12V} \qquad [21.\ 6]$$

The comparator waveform is the desired control waveform required for Boost converter switching duty cycle control. The behavior is a consequence of the "straight-line" relationship of the right triangles from the origin of the sawtooth to the peak, or termination voltage value. The ratio of the V_{fb} to V_{Peak} voltages is proportional to the comparator T_{ON} switching time to T_S pulse oscillator period. We control the comparator duty cycle by establishing the feedback voltage as a proportion of the peak voltage. Conversely, the Slope ratio of voltages provides the "small signal gain" of the modulator.

We have variations of the PWM scheme that we will employ for the duty-cycle control of the Boost converter. First, we scale the sawtooth slope changing its peak magnitude, and consequently scale the requisite feedback voltage to a fraction of the voltages shown:

$$D = \frac{V_{fb}}{V_{Peak}} = \frac{V_{fb}}{Slope \bullet T_S} \qquad [21.\ 7]$$

We introduce the same notation for small-signal quantities that we have used previously to form:

$$D + d = K_{PWM} \bullet \left(V_{fb} + v_{fb}\right) \qquad [21.\ 8]$$

$$K_{PWM} = \frac{1}{Slope \bullet T_S} \qquad [21.\ 9]$$

We subtract the large-signal operating point relationship given in equation [20.8] from the composite of large and small-signal components given in equation [20.9], as follows:

$$\left(D + d\right) - D = d = K_{PWM}\left(V_{fb} + v_{fb}\right) - K_{PWM}V_{fb} = K_{PWM}v_{fb} \qquad [21.\ 10]$$

22.0 The Boost Converter Closed Loop Behavior

We close the Boost converter loop and add a "soft-start" ramp to the V_{Ref} signal so that it takes ~400µsec to reach the desired 28V V_C regulation point. The soft-start feature is included for two primary reasons: first, it controls the input current resulting from initially charging the output capacitor to the operating V_C voltage, and second, it allows the feedback loop to avoid saturation and recovery during the start.

V_{Ref} starts from 12V, and after ~400µsec reaches the desired 28V V_C regulation point. A simple RC filter ensures smooth transitions at the start and finish of the transition.

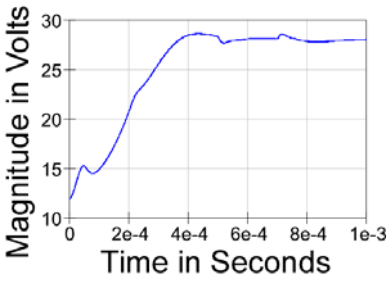

Figure 22.0 Boost Converter Voltage-Mode Tracking

In figure 22.0, we see the V_C output in blue. The RC filter applied to the V_{Ref} signal effectively prevents sudden tracking changes.

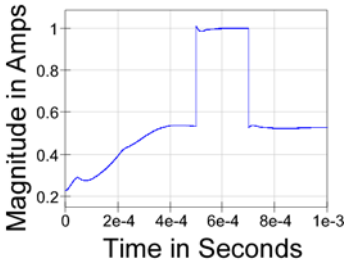

Figure 22.1 Boost Converter Voltage-Mode Load Current

We initiated "soft-start" ramp to the V_{Ref} signal and include an R_{LOAD} = 56 Ω value so that the Boost converter starts under load and is delivering 0.5 Ampere following startup. At the 500 µsecond mark, we apply the full R_{LOAD} = 28 Ω so that the Boost converter is required to deliver 1.0 Ampere for 200 µseconds before returning to half load. We make this step load

change so that we can investigate the transient behavior of the loop as a load is applied and removed.

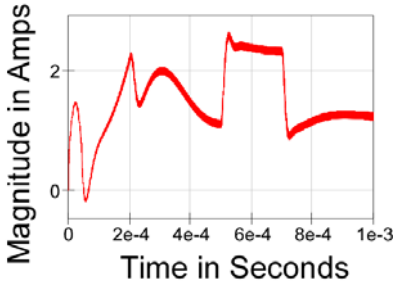

Figure 22.2 Boost Converter Voltage-Mode Inductor Current

During the "soft-start" ramp the inductor current follows the derivative of the V_C output voltage and charges the output capacitor, as well as delivering the 0.5 Ampere to the R_{LOAD} = 56 Ω. The "soft-start" ramp to the V_{Ref} signal terminates at ~400 μsecond and the inductor current decreases supplying the remaining charge to bring the capacitor V_C to a full charge. Thereafter, the inductor current (with its superimposed ripple) is providing the average load current. With a load step at 500 μseconds, and its removal at 700 μseconds, the inductor current responds to the controller signals.

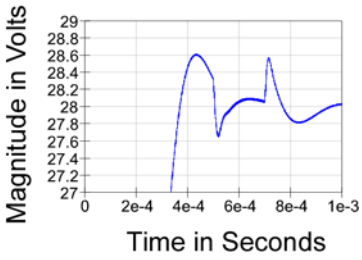

Figure 22.3 Buck Converter Load Effects on the V_C Output Voltage

The change of R_{LOAD} from 56 Ω to R_{LOAD} = 28 Ω and back to R_{LOAD} = 56 Ω causes a rapid change in the V_C voltage. The change from the 0.5 Ampere load to a 1.0 Ampere load at 500 μsec is initially supplied from the charge stored in the output capacitor. As soon as the capacitor voltage decreases though, an error voltage develops and the error amplifier causes the feedback to correct the output error back to the V_C value of 28V.

Similarly, the inductor current change from a 1.0 Ampere load back to a 0.5 Ampere load at 700 µsec must initially be absorbed into the capacitor, charging it to a higher voltage. As soon as the capacitor voltage increases, the error voltage developed at the error amplifier causes the feedback to correct the voltage back to the target $\boldsymbol{V_C}$ value of 28V.

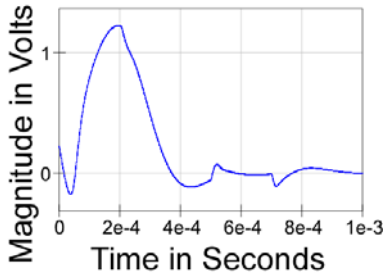

Figure 22.4 Boost Converter Load Error Voltage

The error amplifier causes the feedback to correct the $\boldsymbol{V_C}$ voltage error to zero. Error is correlated with changes in the state variables, Because the $\boldsymbol{V_C}$ voltage error is the source of feedback, the voltage error is associated with changes in the second state variable, the $\boldsymbol{I_L}$ inductor current. We see that there is a "tracking" error difference during the first ~400 µseconds that is required to bring the Boost converter to its required average $\boldsymbol{I_L}$ inductor current. at $\boldsymbol{V_C}$ = 28V with the $\boldsymbol{R_{LOAD}}$ = 56 Ω value. At 500 µseconds and again at 700 µseconds there are the changes in $\boldsymbol{R_{LOAD}}$ and $\boldsymbol{V_C}$ that cause new error voltages to be developed and changes in average $\boldsymbol{I_L}$ inductor current.

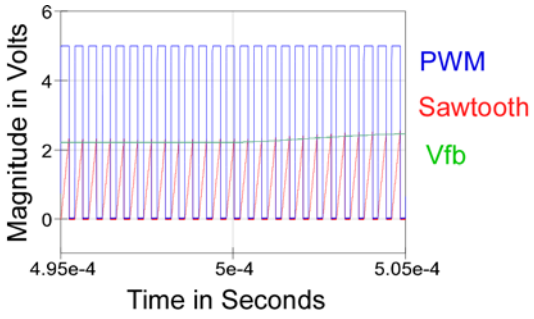

Figure 22.5 Boost Converter Switching Voltage Waveforms

The Boost converter closed-loop responds to the error signals by temporarily increasing or decreasing the average voltage difference across the inductor and consequently its average current. At the increase in load current and consequent decrease in output $\boldsymbol{V_C}$ voltage, the

feedback loop responds by momentarily causing a longer PWM waveform to change to a higher inductor voltage to increase the inductor current. Likewise, at the decrease in load current and consequent increase in output V_C voltage, the feedback loop responds by momentarily forcing a lower average inductor voltage to increase the inductor current.

Under sudden load increase, a $V_{\text{-feedback}}$ signal to the PWM increases so that the PWM the duty cycle becomes longer for several cycles, hence the inductor voltage is at its maximum value equal to the difference between the supply voltage and the V_C voltage for a longer time.

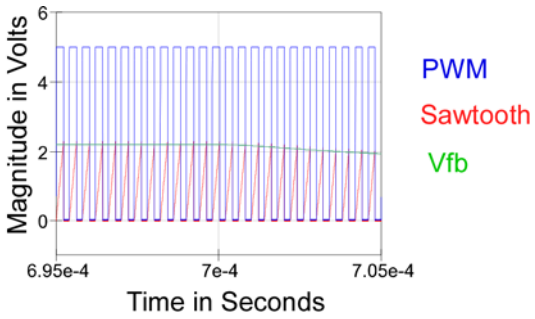

Figure 22.6 Boost Converter PWM Switching Voltage Waveform at Load Decrease

Under sudden load decrease, a $V_{\text{-feedback}}$ signal to the PWM decreases so that the PWM duty cycle becomes shorter for several cycles, hence the inductor voltage is at its minimum value equal to the $-V_C$ voltage for a longer time.

During the sudden application and the sudden removal of the step load, the error may be sufficient to cause T_{Max} or T_{Min} duty cycle in response and the maximum rate of change of inductor current occurs. Because the duty cycle values are limited at the maximum or minimum for some number of cycles, the loop has no feedback control and is operating "open-loop" for a short time. During the open-loop" interval, the integrator still attempts to exert control over the PWM, but succeeds only in accumulation a signal that must be "unwound" before the duty-cycle control is again valid. More complex controllers can be constructed to limit the integrator from accumulating such values and hasten the recovery time.

23.0 Boost Converter with Feed-Forward and Feedback Control Mechanisms

We introduced the requirements for optimal feedforward control in equation [15.3], but found that a right-half plane pole was required. We ignore the frequency dependence and introduce a sub-optimal feedforward control instead. In figure 23.0, we illustrate the combination in the Block Diagram Schematic, as follows:

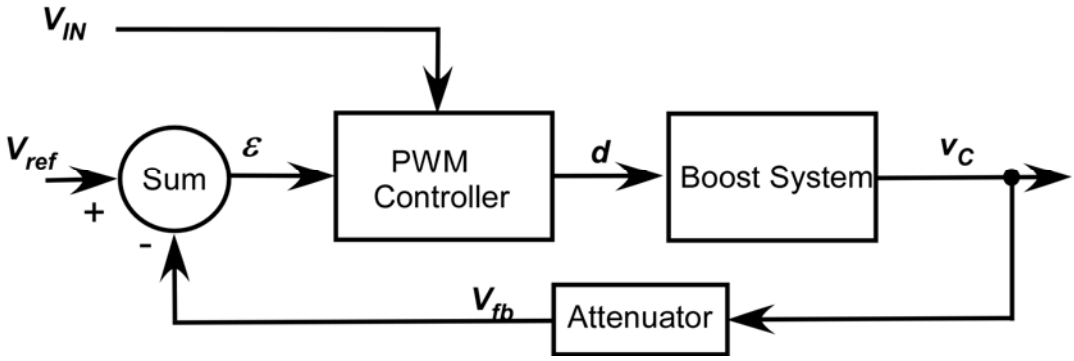

Figure 23.0 Boost Converter Small-Signal Feed-Forward/Feedback Controller

$$d_{ff} = -D\frac{v_{IN}}{V_{IN}} \qquad [23.0]$$

In place of equation [15.3], we introduce equation [23.0], a relationship to reduce the small-signal v_{IN} supply perturbation effects on the output voltage. We show that the PWM can be modified to produce the correction directly. To develop the modifications we revisit the PWM schematic and waveforms.

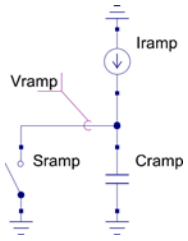

Figure 23.1 Modified Simple Sawtooth Oscillator Schematic

The slope is modified to be given by:

$$Slope = \frac{dV_{ramp}}{dt} = \frac{I_{ramp}}{C_{ramp}} = \frac{G_{SLope}}{C_{ramp}}V_{IN} \qquad [23.1]$$

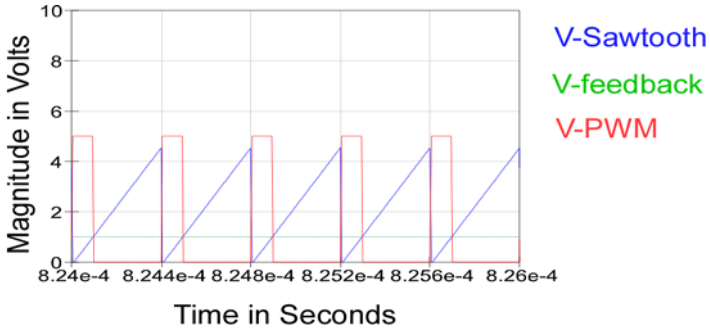

Figure 23.2 Pulse Width Modulation (PWM) Discussion Waveforms

The large-signal duty-cycle signal produced by the PWM is:

$$D = \frac{C_{Ramp}}{G_{Slope} \bullet T_S} \frac{V_{fb}}{V_{IN}} \qquad [23.\ 1]$$

We include small-signal superposition as follows:

$$D + d = \frac{C_{Ramp}}{G_{Slope} \bullet T_S} \bullet \frac{\left(V_{fb} + v_{fb}\right)}{\left(V_{IN} + v_{IN}\right)} \qquad [23.\ 2]$$

$$D + d = \frac{C_{Ramp}}{G_{Slope} \bullet T_S} \bullet \left[\frac{V_{fb}}{\left(V_{IN} + v_{IN}\right)} + \frac{v_{fb}}{\left(V_{IN} + v_{IN}\right)} \right] \qquad [23.\ 3]$$

Performing long division in the first term and eliminating higher-order terms, we have:

$$D + d = \frac{C_{Ramp}}{G_{Slope} \bullet T_S} \left[\left\{ \frac{V_{fb}}{V_{IN}} - \frac{V_{fb}}{V_{IN}} v_{IN} \right\} + \frac{v_{fb}}{V_{IN}} \right] \qquad [23.\ 4]$$

We subtract the large-signal contribution as follows:

$$D + d - D = \frac{C_{Ramp}}{G_{Slope} \bullet T_S} \left[\left\{ \frac{V_{fb}}{V_{IN}} - \frac{V_{fb}}{V_{IN}} v_{IN} \right\} + \frac{v_{fb}}{V_{IN}} \right] - \frac{C_{Ramp}}{G_{Slope} \bullet T_S} \bullet \frac{V_{fb}}{V_{IN}} \qquad [23.\ 5]$$

$$d = \frac{C_{Ramp}}{G_{Slope} \bullet T_S} \left[-\frac{V_{fb}}{V_{IN}} v_{IN} + \frac{v_{fb}}{V_{IN}} \right] = d_{fb} + d_{ff} \qquad [23.\ 6]$$

The resulting PWM relationships provide a capability to add small-signal feedforward control using the v_{IN} term to the feedback control using the v_{Ref} term.

$$d_{fb} = \frac{C_{Ramp}}{G_{Slope} \bullet T_S} \bullet \frac{1}{V_{IN}} v_{\mathrm{Re}\, f} \qquad [23.\ 7]$$

$$d_{ff} = -\frac{C_{Ramp}}{G_{Slope} \bullet T_S} \bullet \frac{V_{fb}}{V_{IN}} v_{IN} \qquad [23.\ 8]$$

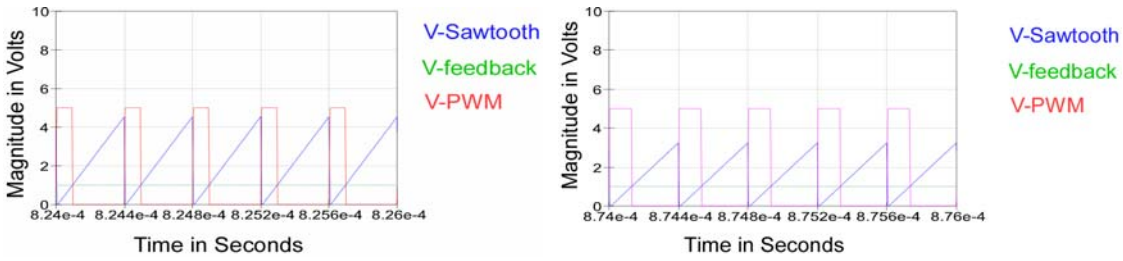

Figure 23.3 Maximum and Minimum Feedforward Slope Dependence on V_{IN}

In figure 32.2, we see that the addition of the slope dependence effectively modifies the duty-cycle with a constant $V_{\text{-feedback}}$ voltage value. Although we cannot infer that the magnitude is optimum, it does alter the PWM duty-cycle in the correct direction to provide some feedforward control.

24.0 Boost Converter Feed-Forward Improvement

In figure 24.0, we show the waveform associated with the introduction of a 2V 10kHz sinusoidal perturbation added to the previously quiet V_{IN} 12V supply as follows:

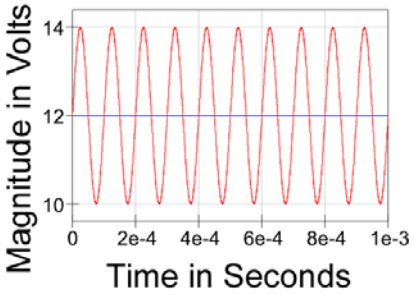

Figure 24.0 Boost Converter V_{IN} with 2V 10kHz AC Perturbation

In figure 24.1, we have added the 10kHz Sinewave to the nominal 12V V_{IN} input without the benefit of feedforward and obtained the responses shown below:

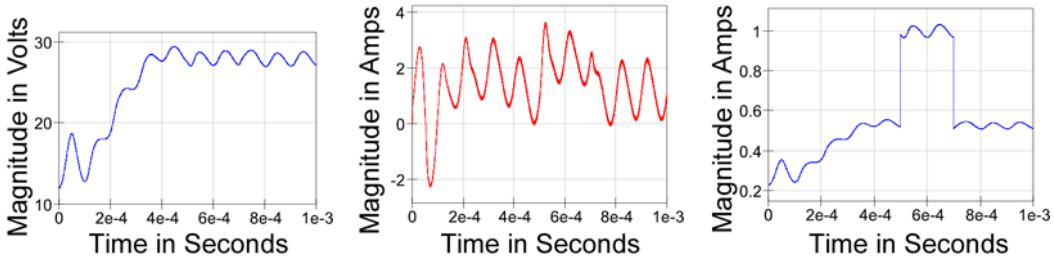

Figure 24.1 V_C , I_L, and I_{Load} Response to V_{IN} with 2V, 10kHz Sinusoid Perturbation

As shown in figure 24.1, the Boost converter running closed-loop converts the V_{IN} input to the V_C output with the ratio determined by the feedback duty-cycle D value. The V_{IN} input perturbation is 4V peak-to-peak, and the response at the V_C output is ~2V peak-to-peak. The Boost converter generates the nominal 28V V_C output from a nominal 12V V_{IN} input, so we should expect an open-loop system to generate a disturbance with the ratio 28/12 * 4V peak-to-peak or > 8V peak-to-peak disturbance disturbance about 4X to ~2V peak-to-peak. The closed-loop feedback is responsible for reducing the disturbance about 4X to ~2V peak-to-peak. The result is consistent with a loop-gain magnitude at 10kHz of ~4, and is about all that can be expected of the compensated feedback loop we have employed.

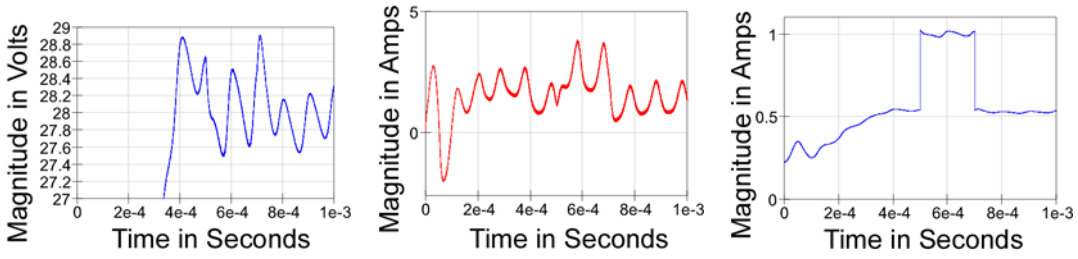

Figure 24.2 V_C , I_L, and I_{Load} Feedforward Response to V_{IN} with 2V, 10kHz Sinusoid Perturbation

We add the modification to the PWM ***Slope*** to make the ***Slope*** current equal $G_{Slope}*V_{IN}$, and obtained a sawtooth with modified ***Slope*** and consequent feedforward as shown in figure 24.2 above with a modest reduction in the disturbance on the V_C output from about 4X at ~2V peak-to-peak about 40X to ~0.2V peak-to-peak. The feedforward control is perhaps sub-optimal, but nonetheless effective.

25.0 Summary and Conclusions

We have introduced a Switchmode Boost power conversion topology and shown considerations for selecting inductor and capacitor components essential for efficient energy transfer.

We analyzed the topologies for two states of switching and produced a state-space averaged model. We extracted a small-signal model and developed a linear model to examine potential stability issues. We included Zero-Order Hold (ZOH) effects of the discrete-time nature of the switch within the control loop, including extra phase contributions and the "notch" behavior near the Nyquist frequency. We designed a Pole-Zero (PZ) compensator necessary to stabilize the open-loop characteristics of the converter with disparate operating points.

We introduced a Pulse-Width Modulator (PWM) and introduced it into the feedback loop. We added feedforward and feedback capabilities to the PWM and contrasted the efficacy of adding feedforward control to a feedback loop.

We have shown that a Boost converter can be designed using voltage feedback to meet the desired specifications.

A more complete design would also consider development of voltage reference components, power switching components, amplifier designs, supervisory startup circuits, component costs, and efficiency effects of component selection, but are beyond the scope of this course. The material covered should enable a working engineer to construct a stable Boost converter using voltage control.

