Switchmode Buck Power Converter Using Voltage-Mode Control

By

Raymond L. Barrett, Jr., PhD, PE
CEO, American Research and Development, LLC

1.0 Switchmode Buck Power Converter Introduction and Basic Model

This course develops models of the Buck converter with duty cycle control. Basic operation, a practical set of examples, and large/small signal models are discussed. Considerations for feedforward control to address line regulation and feedback control to address load regulation of the converter are included.

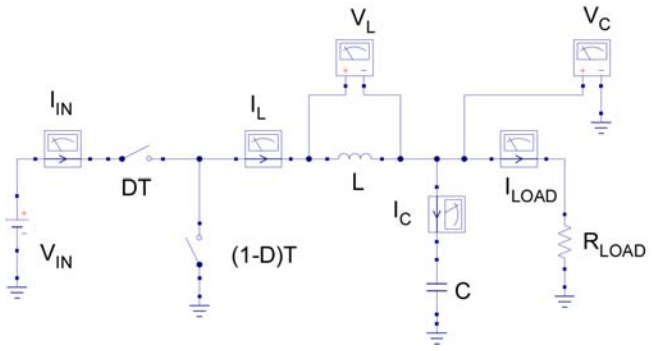

Figure 1.0 Ideal Buck converter schematic

We develop a constant frequency, continuous current Buck converter design, with the switching period defined below in figure 1.1 by $T_2 - T_0 = T$. The converter has two conducting states defined by periods $T_1 - T_0 = DT$ and $T_2 - T_1 = (1 - D)T$, corresponding to the two switching states. The V_{IN} supply is connected with the duty cycle D, and a complement controlled synchronous switch is applied to the complete the connection during the remaining $(1 - D)$ portion of the period.

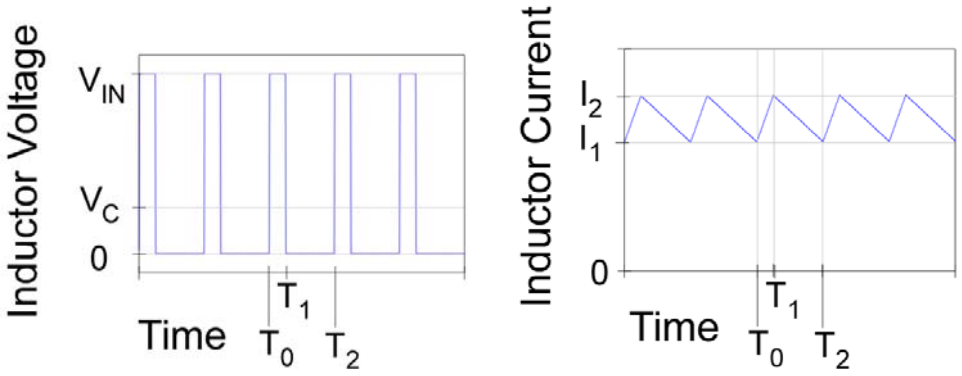

Figure 1.1 Buck converter Inductor operating waveforms

The inductor cannot support a DC voltage difference across its terminals. Instead, any short-term V_L voltage difference results in a constant rate of change of current I_L through the inductor. With some V_C voltage on the capacitor, the inductor has a voltage difference $V_{IN} - V_C$ applied during the DT interval and $-V_C$ applied during the $(1 - D)T$ interval. Overall, we can equate the volt-second products and keep a zero voltage average as:

$$(V_{IN} - V_C)DT - V_C(1 - D)T = 0 \qquad [1.0]$$

$$V_C = DV_{IN} \qquad [1.1]$$

Equation [1.1] provides the basic property of the Buck converter that shows that a lower output voltage V_C can be obtained from the input V_{IN} voltage by controlling the duty cycle D.

2.0 Switchmode Buck Power Converter Input/Output Current Waveforms

As shown in figure 2.0 below, the I_{IN} input current is discontinuous and is non-zero for the DT intervals similar to the time between $T_1 - T_0 = DT$.

During the $T_2 - T_1 = (1 - D)T$ and similar intervals the inductor current flows in the second synchronous grounding switch, rather than the input switch. During these periods, the input current is considered to be identically zero in the ideal schematic, but may consist of leakage, and transient waveforms in a practical circuit.

The I_{LOAD} output current is continuous and flows through the R_{LOAD} resistor as a combination of currents from the inductor and the capacitor. Because the capacitor cannot support a continuous current, but does sink/source AC and transient currents, the average current to the load is identical to the average I_L inductor current.

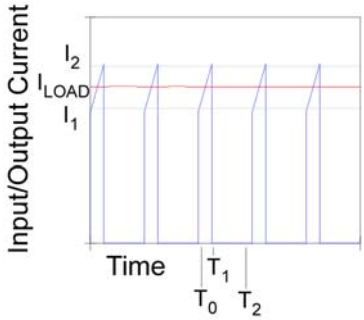

Figure 2.0 Buck converter Input and Output Current waveforms

The average input current during the $T_1 - T_0 = DT$ interval is identical to the I_{LOAD} output current, but because it is non-zero only during that interval, its average value is DI_{LOAD} over each entire period.

3.0 Switchmode Buck Power Converter Input/Output Power and Efficiency

We can calculate the average input power from the product of the input V_{IN} supply times the average DI_{LOAD} input current as follows:

$$P_{IN} = V_{IN} \bullet DI_{LOAD} \qquad [3.0]$$

Similarly, we can calculate the average output power from the product of the output V_C output times the average I_{LOAD} output current as follows:

$$P_{OUT} = V_C \bullet I_{LOAD} \qquad [3.1]$$

If we insert equation [1.1] for the value of V_C in terms of the V_{IN} input voltage into equation [3.1], we find that the input and output average power levels are identical:

$$P_{OUT} = DV_{VIN} \bullet I_{LOAD} = P_{IN} \qquad [3.2]$$

The indicated 100% efficiency is not correct because we have not accounted for losses in the switching elements, or the non-ideal practical components that we must use to implement the design, however, very high efficiencies are achievable, often exceeding 90% efficiency in a practical design.

It is the high efficiency of the switch-mode power converters that accounts for the interest, despite the complexities of the design and control means required to implement a practical design.

4.0 Output Load Current Range

The worst-case, highest current is determined by the smallest R_{LOAD} value, and in turn, the highest I_{LOAD} value. The current handling capacity of the switching devices must be sufficient to support switching the maximum I_{LOAD} value with sufficient speed to support the switching for both DT and $(1 - D)T$ periods.

The maximum value that the R_{LOAD} resistor may attain may be constrained to determine a minimum I_{LOAD} value. A minimum current value may be employed to ensure continuous load current, and to ensure stability requirements

5.0 Input/Output Ripple Current Effects in Component Value Selection

We see from equation [1.1] that the frequency does not enter directly into the relationship between the input voltage and the output voltage, only the duty cycle ***D*** is directly involved. In figure 1.1, we also see that the inductor current forms a triangular waveform between the I_2 peak current, and the I_1 valley current. The triangular peak-to-peak current is defined to be a "ripple current," and is an AC waveform superimposed on the average or DC inductor current.

From the fundamental differential equation description of the behavior of an ideal inductor we have:

$$V_L = L \bullet \frac{dI_L}{dt} \qquad [5.0]$$

For a regime with relatively short times, relatively large inductor values, and relatively small voltages, we can approximate the relationship with line segments as follows:

$$V_L = L \bullet \frac{\Delta I_L}{\Delta t} \qquad [5.1]$$

And in more useful form:

$$\Delta I_L = I_2 - I_1 = \frac{V_L \bullet \Delta t}{L} \qquad [5.2]$$

From equation [5.2], we see that the "volt*second product" of the applied waveform can be used to determine the triangular "ripple" current between the I_2 and I_1 limits. To ensure continuous operation, we implement the design so that I_1 remains non-zero. We select an inductor value large enough to support the "volt*second product" and satisfy the remaining design parameters.

Also implicit in equation [5.2] and the minimum ripple current is a boundary condition on the capacitor value. From the fundamental differential equation description of the behavior of an ideal capacitor we have:

$$I_C = C \bullet \frac{dV_C}{dt} \qquad [5.3]$$

And in more useful form:

$$\Delta V_C = \frac{I_{C-Pk-to-Pk}}{C} \Delta t = \frac{I_2 - I_1}{C} \Delta t \qquad [5.4]$$

Equation [5.4] offers a value for the peak-to-peak ripple voltage that can be expected to be caused by the choice of capacitor value, time intervals, and ripple currents.

Additional non-ideal parasitic components are needed to describe the power lost in the inductor and capacitor.

6.0 Input/Output Voltage Range Considerations

Practical applications require that we produce a controlled value for $\boldsymbol{V_C}$ over a range of input voltage $\boldsymbol{V_{IN}}$ values.

For instance, automotive applications may require a nominal 12V $\boldsymbol{V_{IN}}$ operation, but be expected to function nominally under a low battery condition below 10V, and also operate with transient $\boldsymbol{V_{IN}}$ values in excess of 52V for a few milliseconds in the case of "load-dump" of highly inductive DC motor and solenoid devices connected to that same battery/alternator system. The $\boldsymbol{V_{IN}}$ range can be >5:1 for some automotive applications.

Similarly, "line-powered" applications may be expected to function correctly with common switching circuitry when powered from 110/220V mains sources. The line-powered ranges may be ~85V from the low-line 110V source, but also as higher than 365V under high-line 220V sourcing. The $\boldsymbol{V_{IN}}$ range can be >4.5:1 for some "line-powered" applications.

Although many applications require a fixed output voltage, there are also applications that require a user-programmed output voltage also, often over a considerable range of values.

The capacitor must withstand the highest expected output voltage under both nominal and transient conditions.

The ratio of the smallest output voltage to the highest input voltage determines the smallest nominal value of duty-cycle required. Likewise, the ratio of the highest output voltage to the lowest input voltage determines the largest value of duty-cycle required.

7.0 Switchmode Buck Power Converter Line/Load Regulation Introduction

Practical applications typically require that we provide a controlled value for $\boldsymbol{V_C}$ despite changes in the input voltage $\boldsymbol{V_{IN}}$. The term "line regulation" is used to describe the resulting effect of that control effort.

Also, practical applications require that we provide a controlled value for V_C despite changes in the load current I_{LOAD}. The term "load regulation" is used to describe the resulting effect of that control effort.

Practical applications use a combined strategy for controlling the duty cycle dependent on both the V_{IN} and the V_C values. That part of the control that uses the V_{IN} value to control the duty cycle is called a "feedforward" control mechanism. That part of the controller that uses the V_C value to control the duty cycle is called a "feedback" control mechanism.

To facilitate each form of control, a detailed small-signal model is developed so that the stability and performance of the control can be determined. If feed-forward control is utilized, it is designed later and applied to the system to modify the model behavior after feedback is developed. However, the feedforward control lessens the changes in V_C that the feedback must deal with, making the feedback design less demanding. It is the feedback control that requires a small-signal model to determine gain and phase margins, as well as any compensation required to stabilize the closed loop behavior.

8.0 Switchmode Buck Power Converter Duty-Cycle Control Model

The Buck converter model is described using two state variables: the inductor current I_L and the capacitor voltage V_C. The input voltage V_{IN} and the load resistance R_{LOAD} are retained to express the input and output dependencies for line and load regulation.

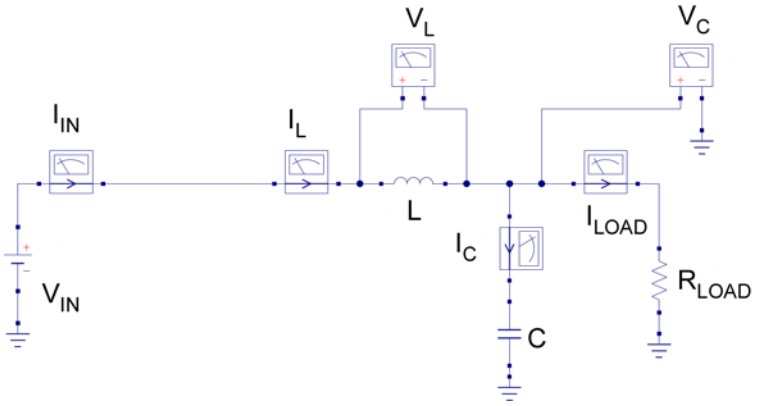

Figure 8.0 Buck converter schematic during the *DT* period

Modeling begins with the topology defined in figure 8.0 during the ***DT*** interval with the input switch conducting and the diode reverse-biased, or OFF. We use Kirchoff's Voltage Law (***KVL***) around the loop including V_{IN}, L, and C, and Kirchoff's Current Law (KCL) at the node defined by the V_C voltage, to write two defining equations:

$$V_{IN} = V_L + V_C \quad [8.0]$$

and

$$I_L = I_{LOAD} + I_C \quad [8.1]$$

Because $\boldsymbol{V_L}$, $\boldsymbol{I_{LOAD}}$, and $\boldsymbol{I_C}$ are not the chosen state variables, we rewrite the equations in terms of the state variables, and use the Laplace "**s**" operator to obtain the equations:

$$V_{IN} = LsI_L + V_C \quad [8.2]$$

and

$$I_L = \frac{V_C}{R_{LOAD}} + CsV_C \quad [8.3]$$

We rewrite into differential equation form, as follows:

$$sI_L = -\frac{1}{L}V_C - \frac{1}{L}V_{IN} \quad [8.4]$$

and

$$sV_C = \frac{1}{C}I_L - \frac{1}{CR_{LOAD}}V_C \quad [8.5]$$

We define a state vector composed of the two state variables:

$$X = \begin{vmatrix} I_L \\ V_C \end{vmatrix} \quad [8.6]$$

We then express the two equations in matrix form using the state vector and build the state matrix as the expression of the two simultaneous equations. It is a matrix differential equation with the derivative of the state vector $\boldsymbol{Xs}$, expressed in terms of the state vector $\boldsymbol{X}$ itself and the $\boldsymbol{V_{IN}}$ input voltage:

$$Xs = \begin{vmatrix} 0 & -1/L \\ 1/C & -1/CR_{LOAD} \end{vmatrix} \bullet X + \begin{vmatrix} 1/L \\ 0 \end{vmatrix} \bullet V_{IN} \quad [8.7]$$

The matrix differential equation [8.7] describes the behavior of the Buck converter during the time $\boldsymbol{DT}$ that the input supply is connected through the closed switch.

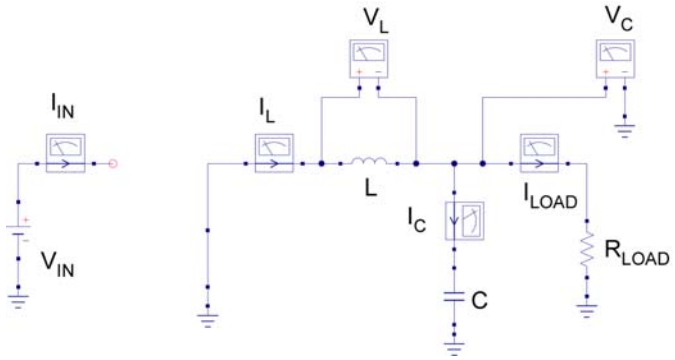

Figure 8.1 Buck converter schematic during the (1-*D*)*T* period

We continue modeling with the topology defined in figure 8.1, with conduction through the synchronous switch during the ***(1-D)T*** interval, again using ***KVL*** and ***KCL*** to write two modified defining equations:

$$0 = V_L + V_C \qquad [8.8]$$

and

$$I_L = I_{LOAD} + I_C \qquad [8.9]$$

As before, we rewrite the defining equations:

$$0 = LsI_L + V_C \qquad [8.10]$$

and

$$I_L = \frac{V_C}{R_{LOAD}} + CsV_C \qquad [8.11]$$

We write equations [8.10] & [8.11] into explicit differential equation form, as follows:

$$sI_L = -\frac{1}{L}V_C \qquad [8.12]$$

and

$$sV_C = \frac{1}{C}I_L - \frac{1}{CR_{LOAD}}V_C \qquad [8.13]$$

Using the state vector as previously defined, we express the new matrix differential equation as follows:

$$Xs = \begin{vmatrix} 0 & -1/L \\ 1/C & -1/CR_{LOAD} \end{vmatrix} \bullet X + \begin{vmatrix} 0 \\ 0 \end{vmatrix} \bullet V_{IN} \qquad [8.14]$$

9.0 Switchmode Buck Power Converter State-Space Average Model

Following the practice of state-space averaging, we sum ***D*** times the component matrix in equation [8.7] plus ***(1-D)*** times the component matrix in equation [8.14] to provide the state-space averaged equations:

$$Xs = D\begin{vmatrix} 0 & -1/L \\ 1/C & -1/CR_{LOAD} \end{vmatrix} \bullet X + D\begin{vmatrix} 1/L \\ 0 \end{vmatrix} \bullet V_{IN}$$
$$+ (1-D)\begin{vmatrix} 0 & -1/L \\ 1/C & -1/CR_{LOAD} \end{vmatrix} \bullet X + (1-D)\begin{vmatrix} 0 \\ 0 \end{vmatrix} \bullet V_{IN} \qquad [9.0]$$

We note that the matrix defined by the components does not change, despite the alteration of the topology caused by switching. The net effect is to modify the source voltage alone as follows:

$$Xs = \begin{vmatrix} 0 & -1/L \\ 1/C & -1/CR_{LOAD} \end{vmatrix} \bullet X + \begin{vmatrix} 1/L \\ 0 \end{vmatrix} \bullet DV_{IN} \qquad [9.1]$$

We will show that the buck converter is much like an Inductor/Capacitor (LC) low pass filter with the source voltage applied to the filter appearing as a duty-cycle modulated waveform that alternates between zero and the full $\boldsymbol{V_{IN}}$ value with the duty-cycle ***D*** during the ON interval. The equivalent input voltage is ***D*** times $\boldsymbol{V_{IN}}$ on average. To make the analogy, we restate our state-space averaged matrix differential equation as simultaneous equations for clarity as follows:

$$sI_L = -\frac{1}{L}V_C + D\frac{1}{L}V_{IN} \qquad [9.2]$$

and

$$sV_C = \frac{1}{C}I_L - \frac{1}{CR_{LOAD}}V_C \qquad [9.3]$$

If we solve equation [9.3] for the inductor current, as follows:

$$I_L = sCV_C + \frac{1}{R_{LOAD}}V_C \qquad [9.4]$$

We can differentiate equation [9.4] and substitute into equation [9.2] for a transfer function, as follows:

$$sI_L = s\left(sCV_C + \frac{1}{R_{LOAD}}V_C\right) = -\frac{1}{L}V_C + D\frac{1}{L}V_{IN} \qquad [9.5]$$

We solve equation [9.5] for the transfer function, as follows:

$$\left(s^2C + \frac{1}{R_{LOAD}}s + \frac{1}{L}\right)V_C = D\frac{1}{L}V_{IN} \qquad [9.6]$$

$$V_C = \left[\frac{1}{LCs^2 + \frac{L}{R_{LOAD}}s + 1}\right]DV_{IN} \qquad [9.7]$$

We see that equation [9.7] is indeed a second-order, LC low pass filter, operating on the average $\boldsymbol{DV_{IN}}$ supply voltage. While this is true, it gives little insight into the dynamics of control of the $\boldsymbol{V_C}$ output voltage by small-signal variations of the duty-cycle.

10.0 A Simple Buck Converter Initial Inductor Choice

We choose as a design requirement; a Buck Converter based on a nominal 10.2V to 14.7V $\boldsymbol{V_{IN}}$ range to supply 3.3V at $\boldsymbol{V_C}$ with 5 milli-Volt maximum ripple voltage. The converter must support a maximum 1 Ampere load. We constrain the minimum load to be 10% of the maximum value, or 100 milli-Amperes, using an internal load resistance. For contrasting illustrations, we begin with a 250 kHz switching frequency.

With a minimum 100 milli-Ampere average load, the peak-to-peak current ripple must be less than 200 milli-Amperes, or the current waveform may become discontinuous, so we choose a 100 milli-Ampere peak-to-peak current ripple as a worst-case value.

From the $\boldsymbol{V_{IN}}$ range and the fixed 3.3V $\boldsymbol{V_C}$ value, we determine that the range of duty-cycle $\boldsymbol{D}$ must be 3.3/14.7 to 3.3/10.2, or 0.22 to 0.33. Knowing the range of the $\boldsymbol{D}$ duty-

cycle interval, we can determine that the ***(1 – D)*** interval is 0.78 to 0.67, and at 250 kHz, the times are 3.12 μsec to 2.68 μsec.

We use the 3.3V V_C value during the longest ***(1 – D),*** or 3.12 μsec, interval to determine the minimum inductor value that will support that voltage with the requisite current change, as follows:

$$0.1 = \Delta I_L = \frac{V_L}{L}\Delta t = \frac{3.3}{L}3.12 \bullet 10^{-6} \qquad [10.0]$$

$$L = \frac{3.3}{0.1} \bullet 3.12 \bullet 10^{-6} = 103\mu H \qquad [10.1]$$

To further address the selection of the inductor, we must consider that the Buck converter delivers a maximum of 1A at 3.3V or 3.3Watts and should not dissipate appreciable power in the inductor, while delivering that current. The inductor must be capable of handling 1A without saturation of the inductance, as well as have a low DC resistance. The power loss in the DC resistance (DCR) of the inductor is:

$$P = I^2 DCR \qquad [10.2]$$

If we evaluate maximum loss in the inductor, that implies:

$$P_{L-Loss} = 1^2 \bullet DCR \qquad [10.3]$$

We find a 150μH Murata component (Digikey # 811-1342-ND) that has 69mΩ and will cause a 2% loss at 1Ampere load current. We consider that as acceptable.

Before proceeding further, we contrast the possibility of operation at a higher switching frequency, notably at 2.5MHz rather than the 250 kHz in the prior calculations.

The range of the ***D*** duty-cycle is unchanged, but the time intervals are shortened by a factor of 10x, so we can determine that the ***(1 – D)*** interval is 0.78 to 0.67, and at 250 kHz, the times are 312 nsec to 268 nsec.

We use the 3.3V V_C value during the longest ***(1 – D),*** or 312 nsec, interval to determine the minimum inductor value that will support that voltage with the requisite current change, as follows:

$$0.1 = \Delta I_L = \frac{V_L}{L}\Delta t = \frac{3.3}{L}312 \bullet 10^{-9} \qquad [10.4]$$

$$L = \frac{3.3}{0.1} \bullet 312 \bullet 10^{-9} = 10.3\mu H \qquad [10.5]$$

The DC resistance requirements are unchanged, but we now find that we can meet the minimum inductance with a 22μH Murata component (Digikey # 811-1341-ND) that has 11mΩ and will cause less than 0.5% loss at 1Ampere load current.

Both inductor choices are from a Digikey on-line catalog and may be obtained from distribution. Other considerations, including price, shielding, assembly requirements, etc., can alter other component parameters, but the inductance and DCR requirements must be met by whatever selection is made

11.0 The Simple Buck Converter Initial Capacitor Choice

We chose to design the example, with a 100 milli-Ampere peak-to-peak current ripple as a worst-case value. We determine the minimum capacitor value from the fundamental capacitor equation:

$$C = \frac{I_2 - I_1}{\Delta V_C} \Delta t \qquad [11.0]$$

The 5 milli-Volt maximum ripple voltage is defined, and we have two cases for the time intervals as follows:

$$C_{250-KHz} = \frac{100 \bullet 10^{-3}}{5 \bullet 10^{-3}} \bullet 3.12 \bullet 10^{-6} = 62.4\mu F \qquad [11.1]$$

$$C_{2.5-MHz} = \frac{100 \bullet 10^{-3}}{5 \bullet 10^{-3}} \bullet 312 \bullet 10^{-9} = 6.24\mu F \qquad [11.2]$$

We can meet the first capacitor requirements with a 6.3V 100 μF Kemet multi-layer ceramic capacitor (Digikey # 399-5620-1-ND), or alternately at the higher frequency with a 6.3V 10 μF Kemet multi-layer ceramic capacitor (Digikey # 399-3029-1-ND). Again, other device parameters must be considered and these selections are for illustration only.

We find that the smaller inductance and capacitance usually are less expensive and constitute one economic argument for higher frequency operation.

12.0 The Simple Buck Converter Initial Component Choices

We have chosen two sets of components to simultaneously meet the ripple current and output ripple voltage constraints, but at 250kHz in one case and 2.5MHz for the other. The component choices determine the second-order, LC lowpass filter, operating on the

average $\boldsymbol{DV_{IN}}$ supply voltage, and the equivalent $\boldsymbol{R_{LOAD}}$ value determines the damping factor of the filter. We express the filter transfer function alone as:

$$T_{LC}(s) = \left[\frac{1}{LCs^2 + \frac{L}{R_{LOAD}} s + 1} \right] \qquad [12.0]$$

In standard form:

$$T_{LC}(s) = \frac{1}{\left(\frac{1}{\omega_0^2} s^2 + \frac{2\varsigma}{\omega_0} s + 1 \right)} \qquad [12.1]$$

From which we obtain:

$$\omega_0 = \frac{1}{\sqrt{LC}} \qquad [12.2]$$

$$\frac{2\varsigma}{\omega_0} = \frac{L}{R_{LOAD}} = 2\varsigma\sqrt{LC} \Rightarrow \varsigma = \frac{1}{2R_{LOAD}} \sqrt{\frac{L}{C}} \qquad [12.3]$$

From the specification to deliver 1 Ampere into the 3.3V output, we determine that:

$$R_{LOAD-Min} = \frac{3.3V}{1A} = 3.3\Omega \qquad [12.4]$$

and also:

$$R_{LOAD-Max} = \frac{3.3V}{0.1A} = 33\Omega \qquad [12.5]$$

Fsw	L	C	ω_0	F_{RES}	ζ_{Max}	ζ_{Min}
250 kHz	150µH	100µF	8.16krad/s	1.30kHz	0.186	0.0186
2.5 MHz	22µH	10µF	67.4 krad/s	10.7kHz	0.225	0.0225

Table 12.0 Example LC Filter Parameters

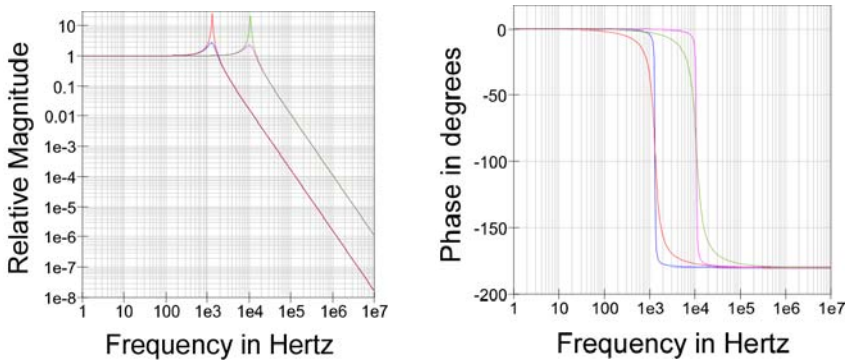

Figure 12.0 LC Filter Magnitude and Phase Bode Plots

We see from figure 12.0 that there is a lightly damped resonance over the entire range of $\boldsymbol{R_{LOAD}}$ values, with considerable resonant peaking as the load gets lighter. Likewise, phase of the transfer function begins with zero degrees and proceeds rapidly to a full 180^{o} phase lag near the resonant frequency. We will see that these characteristics present some issues as we try to control a system with these behaviors.

13.0 Switchmode Buck Power Converter Small-Signal State-Space Average Model

We realize that the LC resonance values due not change, despite the alteration of the topology. We do, however, expect that the input voltage will change, the load will change, and the duty-cycle will be exercised as a control mechanism; the state vector values will change as a consequence.

To model the small-signal behaviors, we introduce a notation that represents a DC operating point with "capital" letters, and small signal perturbations with the smaller letters for each variable and substitute in the model we developed in equation [9.1], as follows:

$$(X+x)s = \begin{vmatrix} 0 & -1/L \\ 1/C & -1/CR_{LOAD} \end{vmatrix} \bullet (X+x) + \begin{vmatrix} 1/L \\ 0 \end{vmatrix} \bullet (D+d)(V_{IN}+v_{IN}) \qquad [13.0]$$

We expand the terms, of equation [13.0], and remove any products of small terms as "second-order" and small enough to ignore, as follows:

$$Xs + xs = \begin{vmatrix} 0 & -1/L \\ 1/C & -1/CR_{LOAD} \end{vmatrix} \bullet X + \begin{vmatrix} 0 & -1/L \\ 1/C & -1/CR_{LOAD} \end{vmatrix} \bullet x - \begin{vmatrix} 0 & -1/L \\ 1/C & -1/CR_{LOAD} \end{vmatrix} \bullet X + \begin{vmatrix} 1/L \\ 0 \end{vmatrix} \bullet DV_{IN} + \begin{vmatrix} 1/L \\ 0 \end{vmatrix} \bullet dV_{IN} + \begin{vmatrix} 1/L \\ 0 \end{vmatrix} \bullet Dv_{IN} - \begin{vmatrix} 1/L \\ 0 \end{vmatrix} \bullet DV_{IN} \quad [13.1]$$

We can solve for the small signal state space averaged model:

$$xs = \begin{vmatrix} 0 & -1/L \\ 1/C & -1/CR_{LOAD} \end{vmatrix} \bullet x + \begin{vmatrix} 1/L \\ 0 \end{vmatrix} \bullet Dv_{IN} + \begin{vmatrix} 1/L \\ 0 \end{vmatrix} \bullet V_{IN} d \quad [13.2]$$

The state-space averaged small-signal model is only valid for small signals. Likewise, it is only valid for small-signal perturbations that are much lower frequency than the switching frequency. Serious aliasing effects can make the model unusable for frequencies approaching a large fraction of the Nyquist frequency (half the switching frequency). However, for analysis at lower frequencies to about 10% of the switching frequency, the state-space averaged model gives good results.

14.0 Small-Signal State-Space Average Model in the Frequency Domain

In classical Laplace form, we can solve the above matrix differential equation [13.2], first for the entire state variable including the inductor current and capacitor voltage followed by the capacitor voltage output alone:

$$\left[sI - \begin{vmatrix} 0 & -1/L \\ 1/C & -1/CR_{LOAD} \end{vmatrix} \right] \bullet x = \begin{vmatrix} 1/L \\ 0 \end{vmatrix} \bullet Dv_{IN} + \begin{vmatrix} 1/L \\ 0 \end{vmatrix} \bullet V_{IN} d \quad [14.0]$$

$$x = \left[sI - \begin{vmatrix} 0 & -1/L \\ 1/C & -1/CR_{LOAD} \end{vmatrix} \right]^{-1} \begin{vmatrix} 1/L \\ 0 \end{vmatrix} Dv_{IN} + \left[sI - \begin{vmatrix} 0 & -1/L \\ 1/C & -1/CR_{LOAD} \end{vmatrix} \right]^{-1} \begin{vmatrix} 1/L \\ 0 \end{vmatrix} V_{IN} d \quad [14.1]$$

$$\left[sI - \begin{vmatrix} 0 & -1/L \\ 1/C & -1/CR_{LOAD} \end{vmatrix} \right]^{-1} = \begin{vmatrix} s & 1/L \\ -1/C & \left(s + 1/CR_{LOAD} \right) \end{vmatrix}^{-1} \quad [14.2]$$

$$\begin{vmatrix} s & 1/L \\ -1/C & \left(s+1/CR_{LOAD}\right) \end{vmatrix}^{-1} = \begin{vmatrix} \dfrac{\left(s+1/CR_{LOAD}\right)}{\left(s^2+\dfrac{s}{CR_{LOAD}}+\dfrac{1}{LC}\right)} & \dfrac{-1/L}{\left(s^2+\dfrac{s}{CR_{LOAD}}+\dfrac{1}{LC}\right)} \\ \dfrac{1/C}{\left(s^2+\dfrac{s}{CR_{LOAD}}+\dfrac{1}{LC}\right)} & \dfrac{s}{\left(s^2+\dfrac{s}{CR_{LOAD}}+\dfrac{1}{LC}\right)} \end{vmatrix} \quad [14.3]$$

$$\left(s^2+\frac{s}{CR_{LOAD}}+\frac{1}{LC}\right)x = \begin{vmatrix} \left(s+1/CR_{LOAD}\right) & -1/L \\ 1/C & s \end{vmatrix} \begin{vmatrix} 1/L \\ 0 \end{vmatrix} Dv_{IN} + \begin{vmatrix} \left(s+1/CR_{LOAD}\right) & -1/L \\ 1/C & s \end{vmatrix} \begin{vmatrix} 1/L \\ 0 \end{vmatrix} V_{IN}d \quad [14.4]$$

$$\left(s^2+\frac{s}{CR_{LOAD}}+\frac{1}{LC}\right)x = \begin{vmatrix} \left(\dfrac{CR_{LOAD}s+1}{LCR_{LOAD}}\right) \\ \dfrac{1}{LC} \end{vmatrix} Dv_{IN} + \begin{vmatrix} \left(\dfrac{CR_{LOAD}s+1}{LCR_{LOAD}}\right) \\ \dfrac{1}{LC} \end{vmatrix} V_{IN}d \quad [14.5]$$

We restate our small-signal equations individually, as follows:

$$\left(s^2+\frac{s}{CR_{LOAD}}+\frac{1}{LC}\right)i_L = \left(\frac{CR_{LOAD}s+1}{LCR_{LOAD}}\right)Dv_{IN} + \left(\frac{CR_{LOAD}s+1}{LCR_{LOAD}}\right)V_{IN}d \quad [14.6]$$

$$\left(s^2+\frac{s}{CR_{LOAD}}+\frac{1}{LC}\right)v_C = \frac{1}{LC}Dv_{IN} + \frac{1}{LC}V_{IN}d \quad [14.7]$$

We restate explicit small-signal equations individually, as follows:

$$i_L = \frac{1}{R_{LOAD}}\left(\frac{CR_{LOAD}s+1}{LCs^2+\dfrac{L}{R_{LOAD}}s+1}\right)Dv_{IN} + \frac{1}{R_{LOAD}}\left(\frac{CR_{LOAD}s+1}{LCs^2+\dfrac{L}{R_{LOAD}}s+1}\right)V_{IN}d \quad [14.8]$$

$$v_C = \frac{1}{\left(LCs^2 + \frac{L}{R_{LOAD}}s + 1\right)} Dv_{IN} + \frac{1}{\left(LCs^2 + \frac{L}{R_{LOAD}}s + 1\right)} V_{IN} d \qquad [14.9]$$

15.0 Feedforward control option for good line regulation

We see that equation [14.9] indicates that the output voltage across the capacitor has a small-signal dependency on both the input voltage $\boldsymbol{v_{IN}}$ and the duty cycle $\boldsymbol{d}$ so that we can force the sum to be zero, as follows:

$$v_C = \frac{1}{\left(LCs^2 + \frac{L}{R_{LOAD}}s + 1\right)} Dv_{IN} + \frac{1}{\left(LCs^2 + \frac{L}{R_{LOAD}}s + 1\right)} V_{IN} d_{ff} = 0 \qquad [15.0]$$

We solve equation [15.0] for:

$$\frac{1}{\left(LCs^2 + \frac{L}{R_{LOAD}}s + 1\right)} Dv_{IN} = -\frac{1}{\left(LCs^2 + \frac{L}{R_{LOAD}}s + 1\right)} V_{IN} d_{ff} \qquad [15.1]$$

$$Dv_{IN} = -V_{IN} d_{ff} \qquad [15.2]$$

$$\frac{d_{ff}}{D} = -\frac{v_{IN}}{V_{IN}} \qquad [15.3]$$

From equation [15.3], we are given a relationship that allows us to eliminate the small-signal supply perturbation effects on the output voltage. We defer the implementation discussion and note only that we will require a pulse width control signal with the characteristics defined in equation [15.3] to provide the requisite effect.

16.0 Feedback control option for good load regulation

From equation [14.9] we retain only the dependency of the capacitor voltage $\boldsymbol{V_C}$ on the duty cycle $\boldsymbol{d}$ as follows:

$$v_C = \frac{1}{\left(LCs^2 + \frac{L}{R_{LOAD}}s + 1\right)} V_{IN} d_{fb} \qquad [16.0]$$

$$\frac{v_C}{d_{fb}} = \frac{1}{\left(LCs^2 + \frac{L}{R_{LOAD}}s + 1\right)} V_{IN} \qquad [16.1]$$

Equation [16.1] expresses the small-signal dependency of the output voltage on the duty-cycle and defers any discussion of how the duty-cycle variation is determined from the feedback.

We construct a typical block diagram for the development of open and closed-loop behaviors as follows:

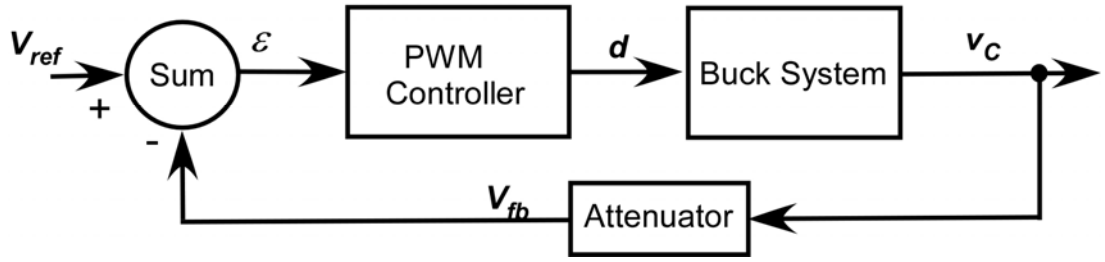

Figure 16.0 Buck Converter Small-Signal Voltage-Mode Controller Block Diagram

The PWM Controller converts the error voltage $\boldsymbol{\varepsilon}$ into the clocking signal with the duty-cycle $\boldsymbol{d}$ for control of the Buck switching. In that respect, $\boldsymbol{\varepsilon}$ is a small-signal quantity itself. The $\boldsymbol{V_{ref}}$ signal is typically a DC value developed from a "Bandgap" or some form of Voltage reference but not necessarily at the same level as the desired output $\boldsymbol{V_C}$ voltage. The "Attenuator" reduces the $\boldsymbol{V_C}$ voltage value so that it can be compared to the $\boldsymbol{V_{ref}}$ value and thus produces the $\boldsymbol{\varepsilon}$ error signal.

We model both the PWM Controller $\boldsymbol{A_{PWM}}$ and the Attenuator $\boldsymbol{A_{ATTEN}}$ as wide-bandwidth gain values to produce an open-loop transfer function:

$$T(s) = A_{PWM} A_{ATTEN} \frac{1}{\left(LCs^2 + \frac{L}{R_{LOAD}}s + 1\right)} V_{IN} \qquad [16.2]$$

In standard form:

$$T(s) = A_{PWM} A_{ATTEN} \frac{1}{\left(\frac{1}{\omega_0^2}s^2 + \frac{2\varsigma}{\omega_0}s + 1\right)} V_{IN} \qquad [16.3]$$

Thus far, our only frequency dependencies lie in the second-order combination of the LC components, but the damping factor ζ depends on the equivalent value of R_{LOAD} on damping the transfer function. From the standard form of the denominator, we have:

$$\omega_0 = \frac{1}{\sqrt{LC}} \qquad [16.4]$$

$$\frac{2\varsigma}{\omega_0} = \frac{L}{R_{LOAD}} = 2\varsigma\sqrt{LC} \Rightarrow \varsigma = \frac{1}{2R_{LOAD}}\sqrt{\frac{L}{C}} \qquad [16.5]$$

We have visited the salient frequency dependencies based on the example values, but restate them here for convenience:

Fsw	L	C	ω_0	F_{RES}	ζ_{Max}	ζ_{Max}
250 kHz	150µH	100µF	8.16krad/s	1.30kHz	0.186	0.0186
2.5 MHz	22µH	10µF	67.4 krad/s	10.7kHz	0.225	0.0225

Table 16.0 Example LC Filter Parameters

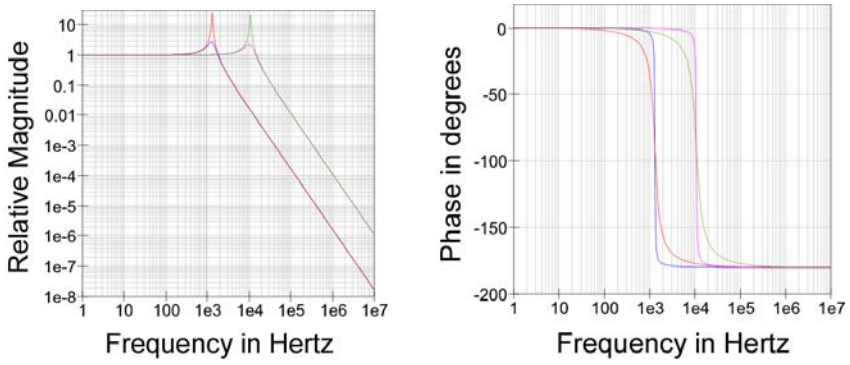

Figure 16.0 LC Filter Bode Plots

17.0 Discrete-Time effects of the Pulse-Width Modulator (PWM)

The Pulse Width Modulator (PWM) block adds a discrete-time sampling effect with an equivalent "Zero-Order-Hold" (ZOH) behavior within the loop. The state-space averaging prevents us from having a result for each cycle of the PWM until each cycle is complete. As a result, we model the PWM ZOH inside the loop, as an average half-cycle delay at the sampling rate, added to each sample.

The ZOH delay behavior adds additional phase delay in the phase response for the loop as follows:

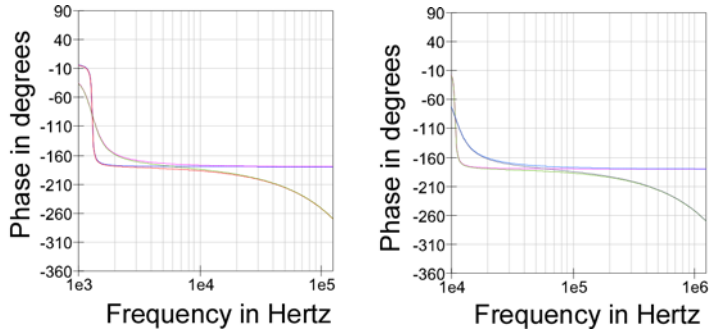

Figure 17.0 LC Filter Phase Plots with and without ZOH Excess Phase

We see that the asymptotic 180^{o} phase shift (shown for reference) above the resonant frequencies cannot be used alone for compensating the phase response of the loop. The ZOH phase must be considered in establishing open-loop stability characteristics such as gain margin and phase margin if fast feedback loops are to be considered.

A second consideration introduced by the ZOH is the magnitude "notch" introduced by the ZOH at the Nyquist frequency. The magnitude envelope is the shape of a "cosine" with the argument equal to the ratio:

$$\left|ZOH\right| = \cos\left(2\pi \frac{f}{f_s}\right) \qquad [17.0]$$

Equation [17.0] introduces a "notch" in the magnitude transfer function at the Nyquist frequency (half the sampling rate), as follows:

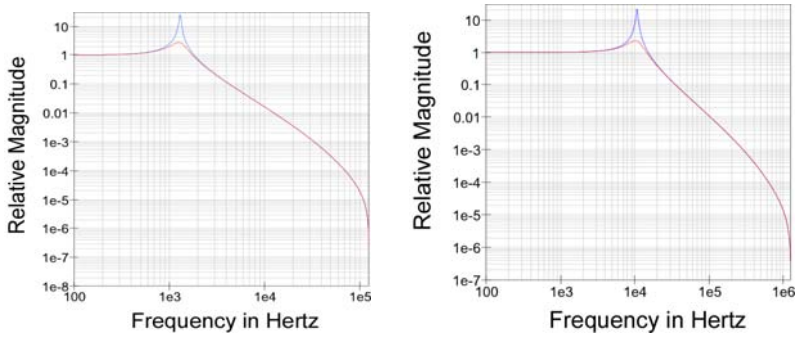

Figure 17.1 LC Filter Magnitude Plots Including Nyquist "Notch" Behavior

We can add gain to the open loop, but must ensure that the net unity-gain frequency crossing occurs at a frequency lower than that with 180° net phase shift. The phase at the unity-gain crossing is the phase margin and we see that this open loop will require some form of compensation to increase that phase margin because we are "uncomfortably" close to 180° net phase shift at all frequencies above the LC resonance frequency for both sets of components.

18.0 Pole-Zero Compensation for the 2.5MHz switching Loop

We have seen that the particular example is composed of an LC behavior with modifications for a Nyquist "notch" and delay, both related to the sampling inherent in the switching/averaging nature of the conversion. These effects notwithstanding, the network is still dominated by the under-damped resonance of the LC components.

The defining LC resonance equation is revisited as follows:

$$T_{LC}(s) = \frac{1}{\left(\frac{1}{\omega_0^2}s^2 + \frac{2\varsigma}{\omega_0}s + 1\right)} \qquad [18.0]$$

The magnitude of the LC resonance equation is given as follows:

$$\left|T_{LC}(j\varpi)\right| = \frac{1}{\sqrt{\left(1-\left(\frac{\varpi}{\omega_0}\right)^2\right)^2 + \left(2\varsigma\frac{\varpi}{\omega_0}\right)^2}} \qquad [18.1]$$

The phase of the LC resonance equation is given as follows:

$$\theta_{LC}(j\varpi) = -\tan^{-1}\left(2\varsigma\frac{\frac{\varpi}{\omega_0}}{1-\left(\frac{\varpi}{\omega_0}\right)^2}\right) \qquad [18.2]$$

We are have shown graphically that the phase below resonance is asymptotically 0°, above resonance is -180°, and precisely -90° at resonance. The rapid rate of change of phase near resonance is problematic for open-loop stability.

The lack of low-frequency gain of the LC filter function requires the addition of substantial DC gain to reap the rewards of the feedback control for error reduction. But, simply adding the gain also increases the unity-gain frequency of the open loop and, with that increase in unity-gain frequency, we also lose phase margin.

Because we propose to add gain, particularly at frequencies lower that the resonant LC frequency, we are forced to compensate for the two-pole rolloff above the LC resonant frequency, as well as the single-pole rolloff of the gain we will add the following PZ compensator:

$$T_{PZ}(s) = \frac{\left(\frac{1}{\omega_{Z1}}s+1\right)\left(\frac{1}{\omega_{Z2}}s+1\right)}{\left(\frac{1}{\omega_{P1}}s+1\right)\left(\frac{1}{\omega_{P2}}s+1\right)\left(\frac{s}{\omega_{Int}}\right)} \qquad [18.3]$$

$$\left|T_{PZ}(j\varpi)\right| = \frac{\sqrt{\left(\frac{\omega}{\omega_{Z1}}\right)^2+1}\bullet\sqrt{\left(\frac{\omega}{\omega_{Z2}}\right)^2+1}}{\sqrt{\left(\frac{\omega}{\omega_{P1}}\right)^2+1}\bullet\sqrt{\left(\frac{\omega}{\omega_{P2}}\right)^2+1}\bullet\left(\frac{\omega}{\omega_{Int}}\right)} \qquad [18.4]$$

$$\theta_{PZ}(j\varpi) = -90^o + \tan^{-1}\left(\frac{\omega}{\omega_{Z1}}\right) + \tan^{-1}\left(\frac{\omega}{\omega_{Z2}}\right) - \tan^{-1}\left(\frac{\omega}{\omega_{P1}}\right) - \tan^{-1}\left(\frac{\omega}{\omega_{p1}}\right) \qquad [18.5]$$

We choose to place the two zero frequencies equal to the LC resonance and place the two pole frequencies two decades above the zeroes. The intention is to use the phase "lead" to compensate for the two-pole "lag" of the LC resonance and defer replacing the two pole "lag" we add until after we reach the unity-gain frequency.

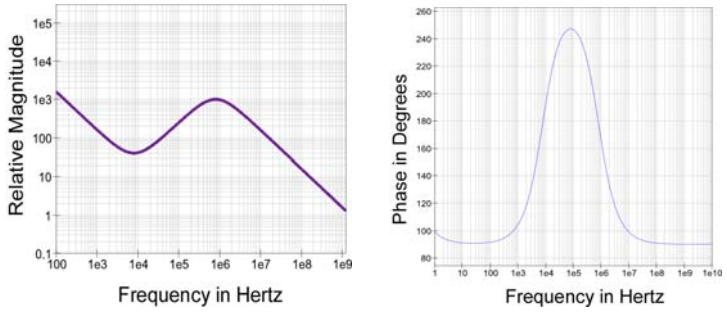

Figure 18.0 Candidate PZ Compensation for 2.5MHz Switching Frequency

We require a single-pole rolloff rate at the open-loop unity-gain frequency for stability. As a consequence, we introduced an integrator for low frequency gain, and a pair of zeroes followed by a pair of poles. We introduce the two zeroes to the integrator function at a frequency near the LC resonant frequency, as indicated in figure [18.0], followed by the zeroes at a frequency higher still. In such a scenario, as the frequency increases from the minimum, the integrator contributes its pole, the LC adds two more and we have a three-pole rolloff rate that we cancel with the two zeroes.

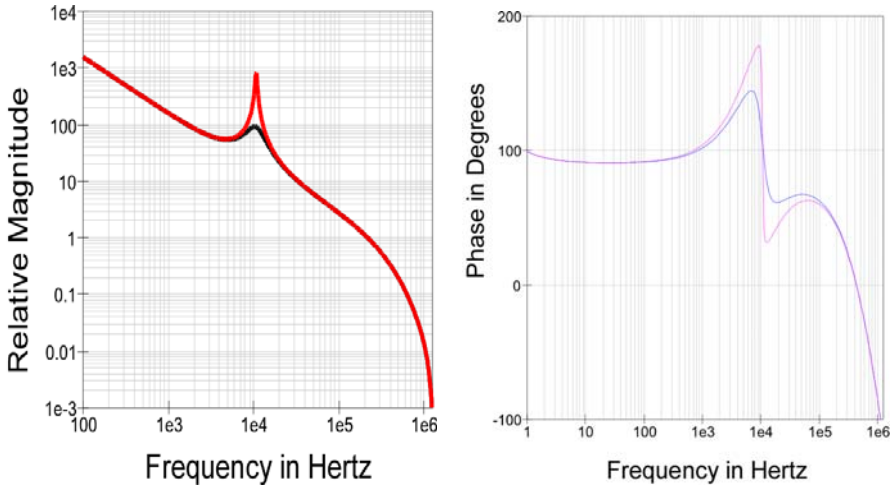

Figure 18.1 LC with Candidate PZ for 2.5MHz Switching Frequency

We see in figure [18.1], that the candidate PZ compensation can be achieved the single-pole rolloff between ~10kHz and ~200kHz, with the unity-gain crossover occurring near ~200kHz.

We cannot allow any three-pole behavior or we will "accumulate" so much phase shift as to make the loop unstable, and as a consequence the two "real" zeroes at the LC resonance reduce the added LC rolloff to a single pole behavior. Unfortunately, with only "real-axis" zeroes there is imperfect phase cancellation as shown above.

With the 200 kHz open-loop unity-gain crossover frequency determined in the figure [18.1] magnitude plot, we see that the phase in figure [18.2] crosses 0^o at a higher frequency and such a loop, if closed, is stable. The approximate phase margin as shown is near 50^o and may show some "ringing" on transient loads.

We consider that the figure 18.0 Pole-Zero (PZ) compensator behavior constrains amplifier selection to devices with unity-gain bandwidth effectively approaching 1 GHz.

A practical PZ compensator realization can be obtained as a cascade of several stages but any additional poles produced in the realization must be well above the 125 kHz open-loop unity-gain frequency shown in figure [18.1] and likewise, not contribute substantial additional phase to the open-loop characteristic shown in figure [18.2].

19.0 Pole-Zero Compensation for the 250kHz switching Loop

Except for the scaling of the frequency axes, the PZ compensator for operation at 250kHz is similar to the approach taken for the 2.5MHz operation.

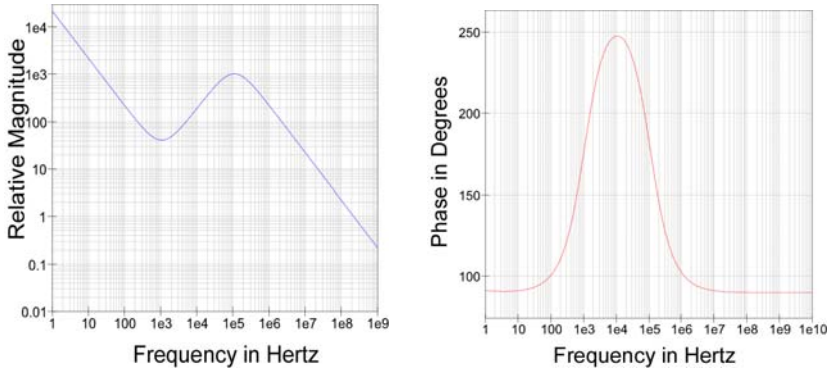

Figure 19.0 Candidate PZ Compensation for 250kHz Switching Frequency

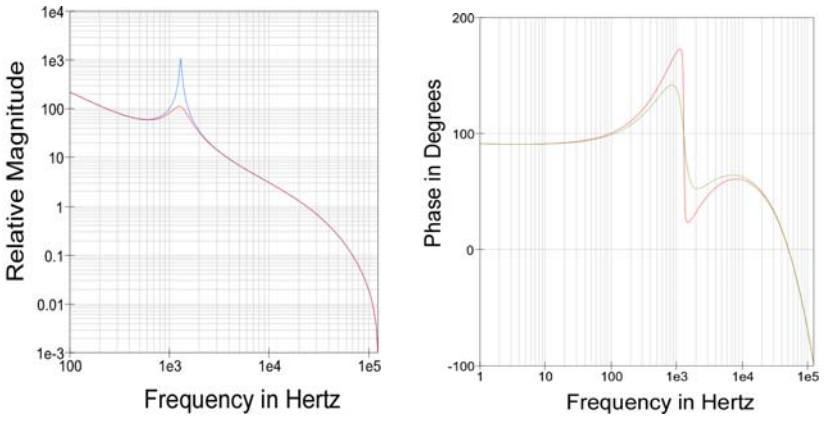

Figure 19.1 LC with Candidate PZ for 250kHz Switching Frequency

We see that this candidate PZ compensation can achieved the single-pole rolloff between ~3kHz and ~30kHz, with the unity-gain crossover occurring at ~25kHz.

With the 25 kHz open-loop unity-gain crossover frequency determined in the figure [19.1] magnitude plot, we see that the phase in figure [19.2] crosses 0^o at a higher frequency and such a loop, if closed, is stable. The approximate phase margin as shown is near 50^o and may show some "ringing" on transient loads.

We shall also see that the requisite behavior constrains whatever amplifier is employed to construct the Pole-Zero (PZ) compensator because a practical amplifier cannot have infinite gain-bandwidth. We see that its unity-gain bandwidth must be effectively in excess of 100 MHz. Again, a cascade compensator design may be employed with similar considerations applied to any new poles introduced and their effects on phase margin.

20.0 Pulse-Width Modulator

It is common practice to use a triangular waveform and a comparator to provide the Pulse-Width Modulation (PWM) function shown in figure 16.0. Various triangular wave shapes have been used from sawtooth to symmetrical triangles, but all translate a voltage at the comparator input into a duty-cycle. We develop the following waveforms:

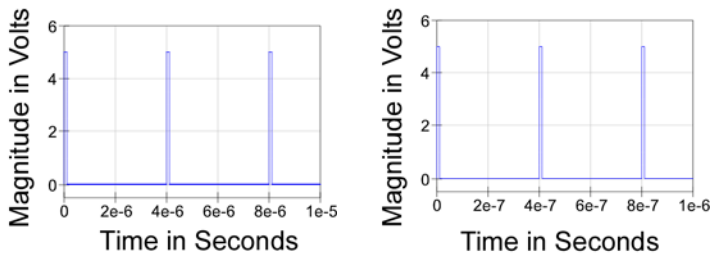

Figure 20.0 Pulse Oscillators at 250kHz and 2.5MHz

We produce a pulse oscillator timing references as short duration pulse trains with the period equal to the T_S sampling period. In these examples, the 250kHz pulse oscillator has a T_S period of 4 microseconds and a duration of ~100 nanoseconds. The 2.5Mhz pulse oscillator is similar, but has a T_S period of 400 nanoseconds and a duration of ~10 nanoseconds.

The pulse oscillators periodically reset a ramp generator and produce typical sawtooth waveforms as follows:

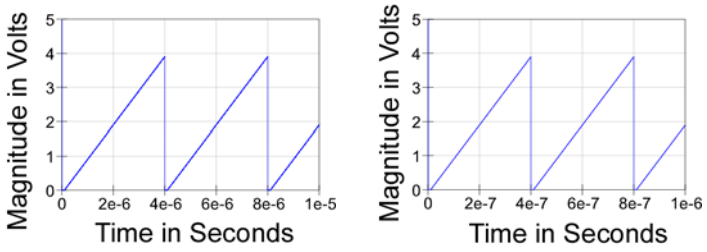

Figure 20.1 Sawtooth Oscillators at 250kHz and 2.5MHz

We obtain the ramp from a current source charging a capacitor and periodically discharge the capacitor to zero volts under control of the pulse oscillator.

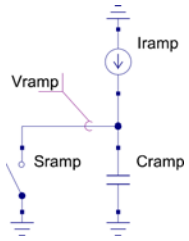

Figure 20.2 Simple Sawtooth Oscillator Schematic

The slope is given by:

$$Slope = \frac{dV_{ramp}}{dt} = \frac{I_{ramp}}{C_{ramp}} \qquad [20.1]$$

For the $\boldsymbol{I_{ramp}}$ current of 1milli-Ampere and a $\boldsymbol{C_{ramp}}$ value of 100 pF, the ***Slope*** is:

$$Slope = \frac{dV_{ramp}}{dt} = \frac{I_{ramp}}{C_{ramp}} = \frac{1 \bullet 10^{-3}}{1 \bullet 10^{-10}} = 10 \frac{V}{\mu \sec} \qquad [20.2]$$

In 400 nsec $\boldsymbol{T_S}$, we attain a 4V signal magnitude and the pulse oscillator resets the capacitor voltage to zero, starting a new cycle at 2.5 MHz.

For the same $\boldsymbol{I_{ramp}}$ current of 1milli-Ampere but a $\boldsymbol{C_{ramp}}$ value of 1000 pF, the slope is:

$$Slope = \frac{dV_{ramp}}{dt} = \frac{I_{ramp}}{C_{ramp}} = \frac{1 \bullet 10^{-3}}{1 \bullet 10^{-9}} = 1 \frac{V}{\mu \sec} \qquad [20.3]$$

It takes a 4 μsec T_S to attain the 4V ramp signal magnitude and the pulse oscillator resets the capacitor voltage to zero, starting a new cycle at 250 kHz.

Using the same charging/discharging circuitry, we can scale the behavior of the sawtooth waveform by choosing different capacitor values.

Similarly, we can also scale the ramp rate ***Slope*** by controlling the charging current. Increasing the current increases the ramp rate, while decreasing the current decreases the ***Slope***. We will revisit the charging current parameter as the primary mechanism for feedforward control to be discussed later.

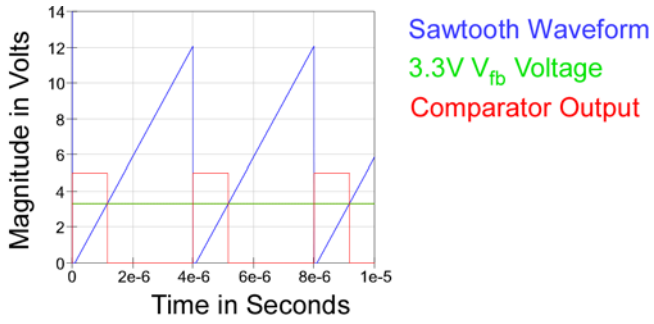

Figure 20.3 Pulse Width Modulation (PWM) Discussion Waveforms

We have taken liberties with the magnitudes in figure 20.3 to enable clarity in the discussions that follow. We have retained the 250kHz T_S timing of a 4 μsec cycle, but scaled the sawtooth peak magnitude to 12V to enable discussions of "similar triangles" in the following discussion. For the example illustrated in figure 20.3, the slope is:

$$Slope = \frac{dV_{ramp}}{dt} = \frac{12V}{4\mu\,\text{sec}} = 3\frac{V}{\mu\,\text{sec}} \qquad [20.4]$$

And, indirectly, the V_{Peak} peak voltage in this case is:

$$V_{Peak} = \frac{dV_{ramp}}{dt} \bullet T_S = 3\frac{V}{\mu\,\text{sec}} \bullet 4\mu\,\text{sec} = 12V \qquad [20.5]$$

At the prescribed 3V/μsec slope, we require 1.1μsec to reach the 3.3V switching point of the comparator set by the 3.3V V_{fb} feedback voltage. It takes the full 4 μsec to reach the 12V V_{Peak} peak value. The comparator output waveform duty cycle is:

$$D = \frac{T_{ON}}{T_S} = \frac{1.1\mu\sec}{4\mu\sec} = 0.275 = \frac{V_{fb}}{V_{Peak}} = \frac{3.3V}{12V} \qquad [20.\ 6]$$

The comparator waveform is precisely the desired control waveform required for Buck converter switching duty cycle control. The behavior is a consequence of the "straight-line" relationship of the right triangles from the origin of the sawtooth to the peak, or termination voltage value. The ratio of the $\boldsymbol{V_{fb}}$ to $\boldsymbol{V_{Peak}}$ voltages is proportional to the comparator $\boldsymbol{T_{ON}}$ switching time to $\boldsymbol{T_S}$ pulse oscillator period. We control the comparator duty cycle by establishing the feedback voltage as a proportion of the peak voltage.

We have variations of the PWM scheme that we will employ for the duty-cycle control of the Buck converter. First, we scale the sawtooth slope changing its peak magnitude, and consequently scale the requisite feedback voltage to a fraction of the voltages shown:

$$D = \frac{V_{fb}}{V_{Peak}} = \frac{V_{fb}}{Slope \bullet T_S} \qquad [20.\ 7]$$

We can modify the constant slope, making the $\boldsymbol{I_{Ramp}}$ charging current proportional to $\boldsymbol{V_{IN}}$, shown above as a constant:

$$D = \frac{V_{fb}}{Slope \bullet T_S} = \frac{V_{fb}}{\frac{I_{Ramp}}{C_{Ramp}} \bullet T_S} = \frac{C_{Ramp}}{I_{Ramp} \bullet T_S} V_{fb} = K_{PWM} \bullet V_{fb} \qquad [20.\ 8]$$

We introduce the same notation for small-signal quantities that we have used previously to form:

$$D + d = K_{PWM} \bullet \left(V_{fb} + v_{fb}\right) \qquad [20.\ 9]$$

We subtract the large-signal operating point relationship given in equation [20.8] from the composite of large and small-signal components given in equation [20.9], as follows:

$$D + d - D = d = K_{PWM}\left(V_{fb} + v_{fb}\right) - K_{PWM} V_{fb} = K_{PWM} v_{fb} \qquad [20.\ 10]$$

21.0 Feedback Open Loop Transfer Function

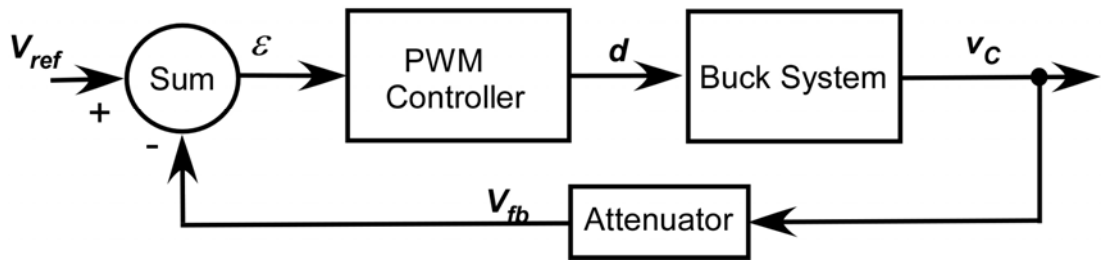

Figure 21.0 Buck Converter Small-Signal Voltage-Mode Control Block Diagram

We cascade all the components to form the "open-loop" transfer function ***T(s)*** as follows:

$$T(s) = K_{Atten} \bullet [T_{PZ}(s) \bullet K_{PWM}] \bullet T_{LC}(s) \qquad [21.0]$$

We previously included the PZ compensator in the PWM to meet "open-loop" transfer function ***T(s)*** stability requirements, therefore, the addition of the attenuator and PWM remaining functions must have a "neutral" effect on stability. We meet that requirement by re-grouping the terms as follows:

$$T(s) = [K_{Atten} \bullet K_{PWM}] \bullet [T_{PZ}(s) \bullet T_{LC}(s)] \qquad [21.1]$$

and we make the condition that:

$$|K_{Atten} \bullet K_{PWM}| = 1 \qquad [21.2]$$

We introduce only sufficient gain into the PWM to offset the attenuation encountered in the feedback attenuator.

22.0 The Buck Converter Closed Loop Behavior

We close the Buck converter loop and add a "soft-start" ramp to the V_{Ref} signal so that it takes ~100µsec to reach the desired 3.3V V_C regulation point. The soft-start feature is included for two primary reasons: first, it controls the input current resulting from initially charging the output capacitor to the operating V_C voltage, and second, it allows the feedback loop to avoid saturation and recovery during the start.

V_{Ref} starts from zero, and after ~100µsec reaches the desired 3.3V V_C regulation point. A simple RC filter ensures smooth transitions at the start and finish of the transition.

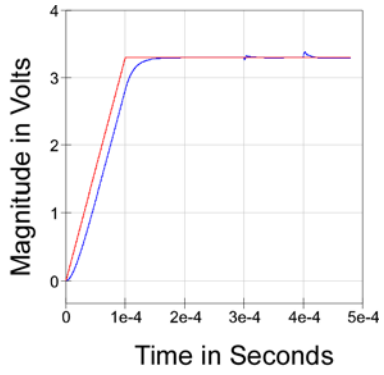

Figure 22.0 Buck Converter Voltage-Mode Tracking

In figure 22.0, we see the $\boldsymbol{V_{Ref}}$ signal in red as well as the $\boldsymbol{V_C}$ output response in blue. The RC filter applied to the $\boldsymbol{V_{Ref}}$ signal effectively prevents sudden tracking changes.

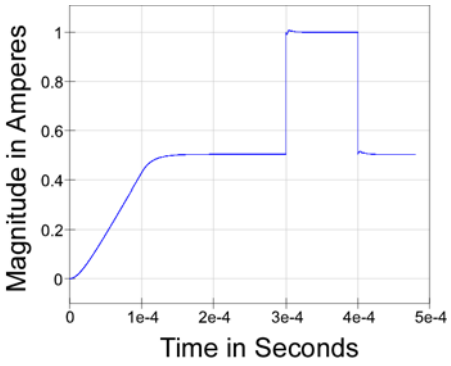

Figure 22.1 Buck Converter Voltage-Mode Load Current

We initiated "soft-start" ramp to the $\boldsymbol{V_{Ref}}$ signal and include an $\boldsymbol{R_{LOAD}}$ = 6.6 Ω value so that the Buck converter starts under load and is delivering 0.5 Ampere following startup. At the 300 µsecond mark, we apply the full $\boldsymbol{R_{LOAD}}$ = 3.3 Ω so that the Buck converter is required to deliver 1.0 Ampere for 100 µseconds before returning to half load. We make this step load change so that we can investigate the transient behavior of the loop as a load is applied and removed.

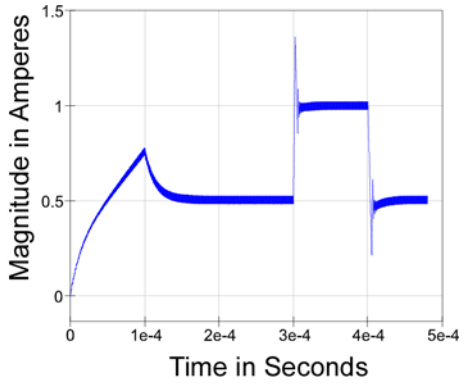

Figure 22.2 Buck Converter Voltage-Mode Inductor Current

During the "soft-start" ramp the inductor current follows the derivative of the V_C output voltage and charges the output capacitor, as well as delivering the 0.5 Ampere to the R_{LOAD} = 3.3 Ω. The "soft-start" ramp to the V_{Ref} signal terminates at ~100 μsecond and the inductor current decreases supplying the remaining charge to bring the capacitor V_C to a full charge at ~200 μsecond. Thereafter, the inductor current (with its superimposed ripple) is providing the average load current. With a load step at 300 μseconds, and its removal at 400 μseconds, the inductor current responds to the controller signals.

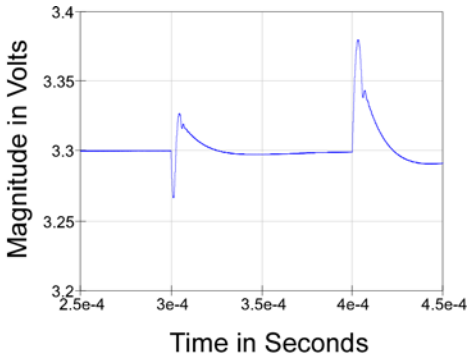

Figure 22.3 Buck Converter Load Effects on the V_C Output Voltage

The change of R_{LOAD} from 6.6 Ω to R_{LOAD} = 3.3 Ω and back to R_{LOAD} = 6.6 Ω causes a rapid change in the V_C voltage. The change from the 0.5 Ampere load to a 1.0 Ampere load at 300 μsec is initially supplied from the charge stored in the output capacitor. As soon as the capacitor voltage decreases though, an error voltage develops and the error amplifier causes the feedback to correct the output error back to the a V_C value of 3.3V.

Similarly, the inductor current change from a 1.0 Ampere load back to a 0.5 Ampere load at 400 µsec must initially be absorbed into the capacitor, charging it to a higher voltage. As soon as the capacitor voltage increases, the error voltage developed at the error amplifier causes the feedback to correct the voltage back to the target $\boldsymbol{V_C}$ value of 3.3V.

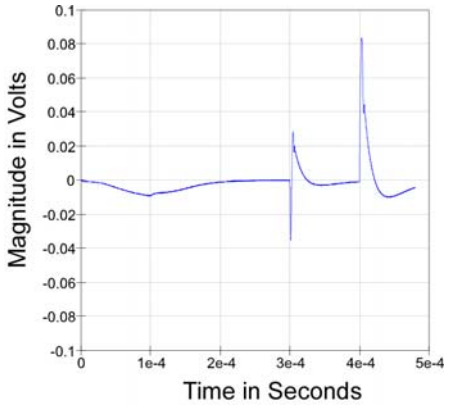

Figure 22.4 Buck Converter Load Error Voltage

The error amplifier that causes the feedback to correct the $\boldsymbol{V_C}$ voltage error to zero until there is no error. Error is correlated with changes in the state variables, Because the $\boldsymbol{V_C}$ voltage error is the source of feedback, the voltage error is associated with changes in the second state variable, the $\boldsymbol{I_L}$ inductor current. We see that there is a "tracking" error difference during the first ~200 µseconds that is required to bring the Buck converter to its required average $\boldsymbol{I_L}$ inductor current. at $\boldsymbol{V_C}$ = 3.3V with the $\boldsymbol{R_{LOAD}}$ = 6.6 Ω value. At 300 µseconds and again at 400 µseconds there are the changes in $\boldsymbol{R_{LOAD}}$ and $\boldsymbol{V_C}$ that cause new error voltages to be developed and changes in average $\boldsymbol{I_L}$ inductor current..

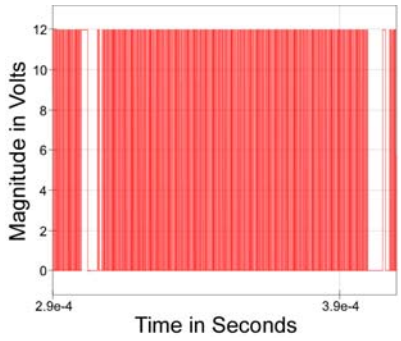

Figure 22.5 Buck Converter Switching Voltage Waveform

The Buck converter closed-loop responds to the error signals by temporarily increasing or decreasing the average voltage difference across the inductor and consequently its average current. At the increase in load current and consequent decrease in output V_C voltage, the feedback loop responds by momentarily causing a change to a higher average inductor voltage to increase the inductor current. Likewise, at the decrease in load current and consequent increase in output V_C voltage, the feedback loop responds by momentarily forcing a lower average inductor voltage to increase the inductor current.

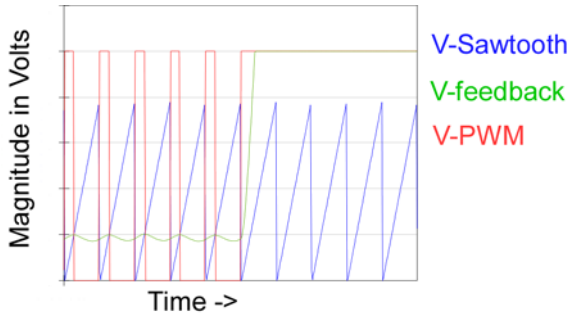

Figure 22.6 Buck Converter PWM Switching Voltage Waveform at Load Increase

Under sudden load increase, a $V_{\text{-feedback}}$ signal to the PWM increases so that the PWM the duty cycle becomes 100% for several cycles, hence the inductor voltage is at its maximum value equal to the difference between the supply voltage and the V_C voltage. No greater increase in voltage is possible so the inductor current increases with its maximum rate of change.

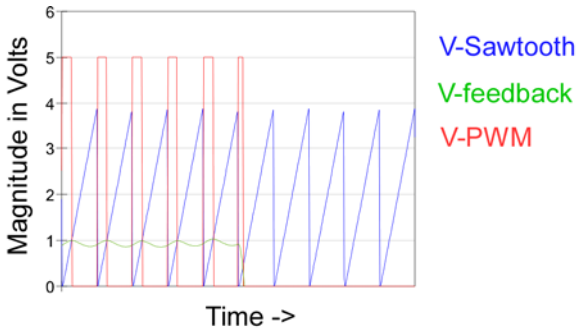

Figure 22.7 Buck Converter PWM Switching Voltage Waveform at Load Decrease

Under sudden load decrease, a $V_{\text{-feedback}}$ signal to the PWM decreases so that the PWM duty cycle becomes 0% for several cycles, hence the inductor voltage is at its minimum

value equal to the $-V_C$ voltage. No greater decrease in voltage is possible so the inductor current decreases with its maximum rate of change.

During the sudden application and the sudden removal of the step load, the error is sufficient to cause 100% or 0% duty cycle in response and the maximum rate of change of inductor current occurs. Because the duty cycle values are saturated at the maximum or minimum for some number of cycles, the loop has no feedback control and is operating "open-loop" for a short time. During the open-loop" interval, the integrator still attempts to exert control over the PWM, but succeeds only in accumulation a signal that must be "unwound" before the duty-cycle control is again valid. More complex controllers can be constructed to limit the integrator from accumulating such values and hasten the recovery time.

23.0 Buck Converter with Feed-Forward and Feedback Control Mechanisms

We introduced the requirements for feedforward control as well as for the open-loop portions of the feedback control. In figure 23.0, we illustrate the combination in the Block Diagram Schematic, as follows:

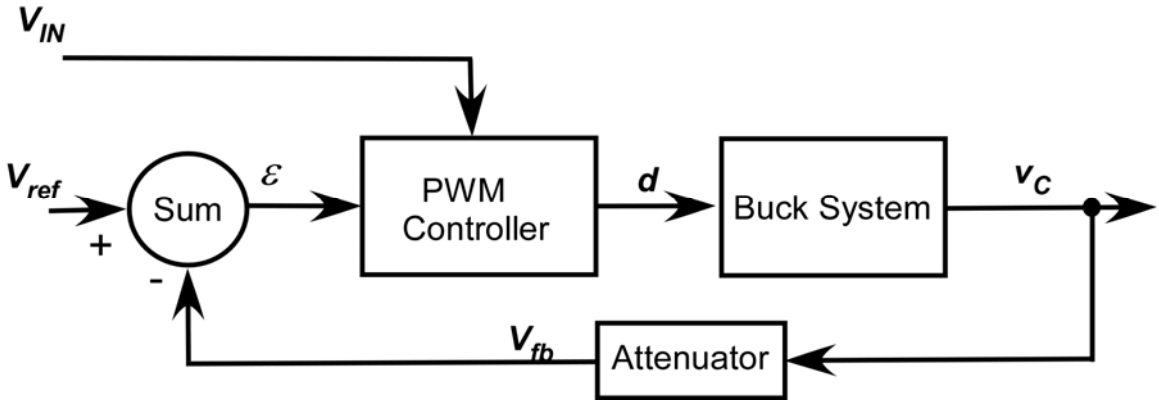

Figure 23.0 Buck Converter Small-Signal Feed-Forward/Feedback Controller

$$d_{ff} = -D\frac{v_{IN}}{V_{IN}} \qquad [23.0]$$

From equation [15.3], reproduced explicitly here as equation [23.0], we deduced a relationship to eliminate the small-signal v_{IN} supply perturbation effects on the output voltage. We show that the PWM can be modified to produce the requisite correction directly. To develop the modifications we revisit the PWM schematic and waveforms.

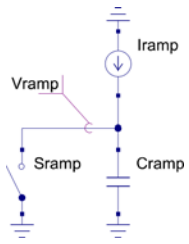

Figure 23.2 Modified Simple Sawtooth Oscillator Schematic

The slope is modified to be given by:

$$Slope = \frac{dV_{ramp}}{dt} = \frac{I_{ramp}}{C_{ramp}} = \frac{G_{SLope}}{C_{ramp}} V_{IN} \qquad [23.1]$$

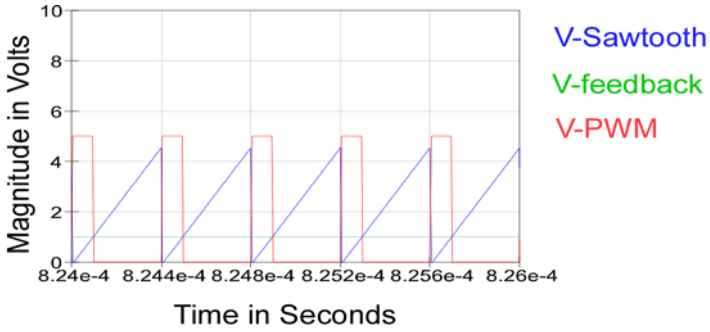

Figure 23.3 Pulse Width Modulation (PWM) Discussion Waveforms

The large-signal duty-cycle signal produced by the PWM is:

$$D = \frac{C_{Ramp}}{G_{Slope} \bullet T_S} \frac{V_{fb}}{V_{IN}} \qquad [23.1]$$

We include small-signal superposition as follows:

$$D + d = \frac{C_{Ramp}}{G_{Slope} \bullet T_S} \bullet \frac{\left(V_{fb} + v_{fb}\right)}{\left(V_{IN} + v_{IN}\right)} \qquad [23.2]$$

$$D + d = \frac{C_{Ramp}}{G_{Slope} \bullet T_S} \bullet \left[\frac{V_{fb}}{(V_{IN} + v_{IN})} + \frac{v_{fb}}{(V_{IN} + v_{IN})} \right] \qquad [23.\ 3]$$

Performing long division in the first term and eliminating higher-order terms, we have:

$$D + d = \frac{C_{Ramp}}{G_{Slope} \bullet T_S} \left[\left\{ \frac{V_{fb}}{V_{IN}} - \frac{V_{fb}}{V_{IN}} v_{IN} \right\} + \frac{v_{fb}}{V_{IN}} \right] \qquad [23.\ 4]$$

We subtract the large-signal contribution as follows:

$$D + d - D = \frac{C_{Ramp}}{G_{Slope} \bullet T_S} \left[\left\{ \frac{V_{fb}}{V_{IN}} - \frac{V_{fb}}{V_{IN}} v_{IN} \right\} + \frac{v_{fb}}{V_{IN}} \right] - \frac{C_{Ramp}}{G_{Slope} \bullet T_S} \bullet \frac{V_{fb}}{V_{IN}} \qquad [23.\ 5]$$

$$d = \frac{C_{Ramp}}{G_{Slope} \bullet T_S} \left[-\frac{V_{fb}}{V_{IN}} v_{IN} + \frac{v_{fb}}{V_{IN}} \right] = d_{fb} + d_{ff} \qquad [23.\ 6]$$

The resulting PWM relationships provide a capability to add small-signal feedforward control using the v_{IN} term to the feedback control using the v_{Ref} term.

$$d_{fb} = \frac{C_{Ramp}}{G_{Slope} \bullet T_S} \bullet \frac{1}{V_{IN}} v_{\mathrm{Re}\, f} \qquad [23.\ 7]$$

$$d_{ff} = -\frac{C_{Ramp}}{G_{Slope} \bullet T_S} \bullet \frac{V_{fb}}{V_{IN}} v_{IN} \qquad [23.\ 8]$$

24.0 Buck Converter with Feed-Forward Control Mechanism Acting Alone

We prepare to illustrate the effects of feedforward control by disabling feedback thus operating the Buck converter open-loop, but near its normal quiescent operating point.

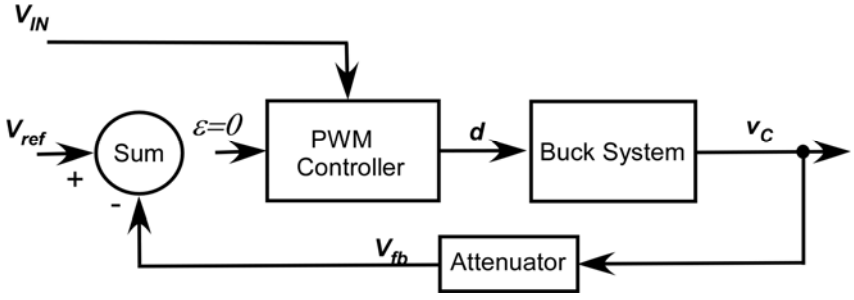

Figure 24.0 Buck Converter with the Feedback Disabled

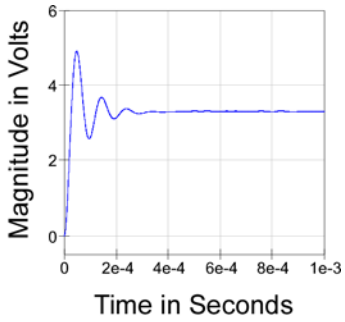

Figure 24.1 Buck Converter Open-Loop V_C Response to a V_{IN} Step

In figure 24.1, we illustrate that the open-loop Buck converter step response exhibits the expected under-damped resonance of the LC filter, although the constant duty-cycle reduces the nominal 12V $\boldsymbol{V_{IN}}$ input to the nominal $\boldsymbol{V_C}$ target 3.3 V output.

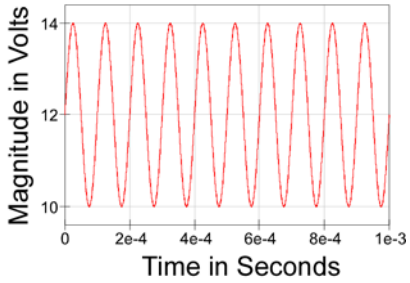

Figure 24.2 Buck Converter V_{IN} Step with 2V 10kHz AC Perturbation

In figure 24.2, we add a 10kHz Sinewave to the nominal 12V $\boldsymbol{V_{IN}}$ input and obtain the response shown in figure 24.3 below:

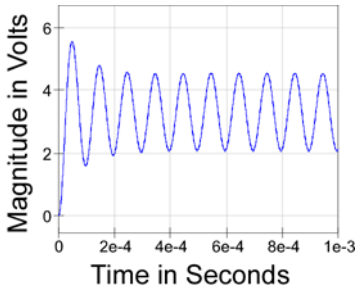

Figure 24.3 Open-Loop V_C Response to V_{IN} Step with Perturbation

As shown in figure 24.3, the Buck converter running open-loop faithfully converts the V_{IN} input to the V_C output with the ratio determined by the constant duty-cycle D value.

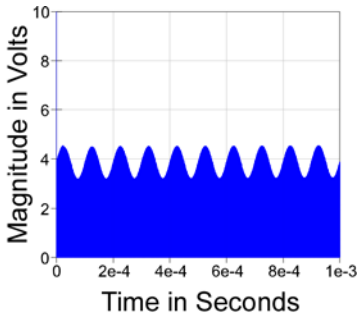

Figure 24.4 Peak Sawtooth "Envelope" with Feedforward Slope Dependence on V_{IN}

We add the modification to the PWM ***Slope*** to make the ***Slope*** current equal $G_{Slope}*V_{IN}$, and obtain a sawtooth with modified ***Slope*** and consequent "modulated" peak value as shown in figure 24.4 above.

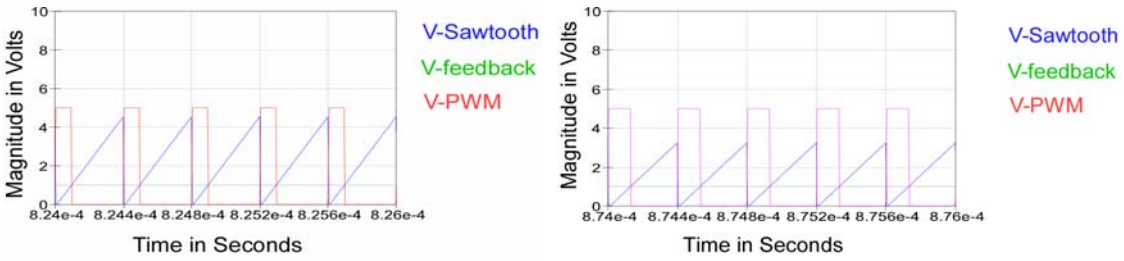

Figure 24.5 Maximum and Minimum Feedforward Slope Dependence on V_{IN}

In figure 24.5, we show details of the sawtooth waveform centered on the 14V maximum V_{IN} value at 825 μsec and the 10 V minimum V_{IN} value centered on 875 μseconds. The duty-cycle shows the required inverse relationship to V_{IN}, being smaller for high values of V_{IN}, and larger for small values of V_{IN}, despite the constant value of 1V for the $V_{F\text{-}feedback}$ signal. We could argue that the range of V_{IN} values from 10V to 14V violates the small-signal assumptions, but we shall see below that the feedforward result is still acceptable in figure 24.6 with the feedforward effect on the V_C voltage, substantially reducing the effects of the AC perturbation on the V_C output voltage using the feedforward control effects.

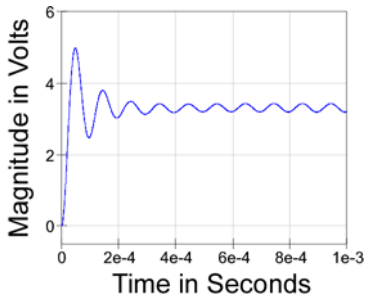

Figure 24.6 Open-Loop V_C Response to V_{IN} Perturbation Using Feedforward Alone

25.0 Buck Converter Adding Feed-Forward to Feedback Control Mechanisms

We contrast the Buck converter with feedback alone versus the combined feed-forward with feedback control as follows:

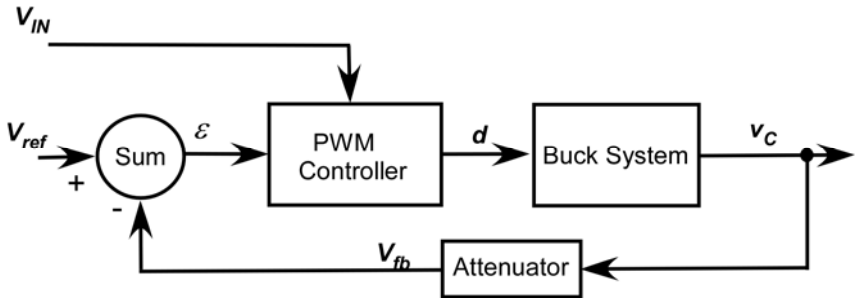

Figure 25.0 Buck Converter Small-Signal Feed-Forward/Feedback Controller

In the following comparisons, we provide the V_{IN} source with AC perturbation, but we contrast the response at the V_C output, as well as internal control signals with feedforward and feedback employed together versus feedback control alone.

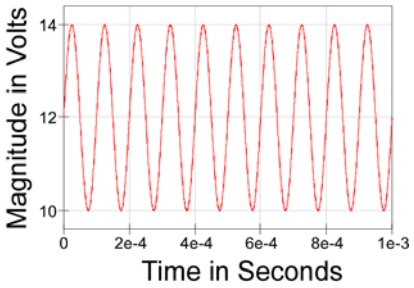

Figure 25.1 Buck Converter V_{IN} with 2V 10kHz AC Perturbation

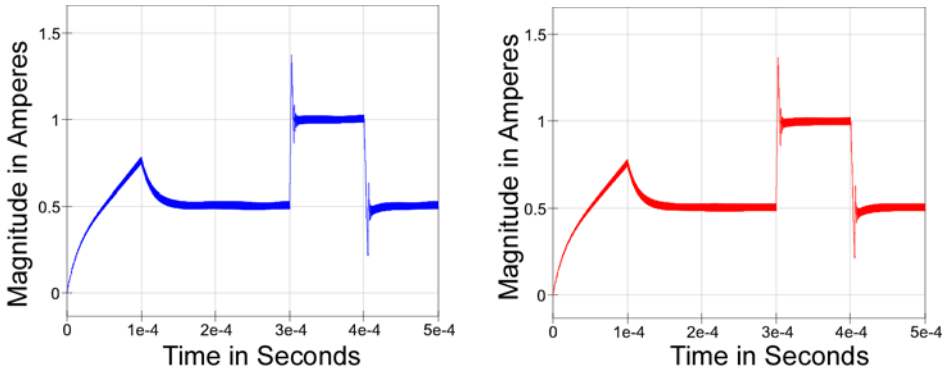

Figure 25.2 Buck Converter Inductor Current with AC Perturbation on V_{IN}

In figure 25.2, we illustrate the inductor current for systems employing feedback alone in the blue trace versus both feedback and feedforward for the red trace. The differences are nearly imperceptible on the relatively large nominal values.

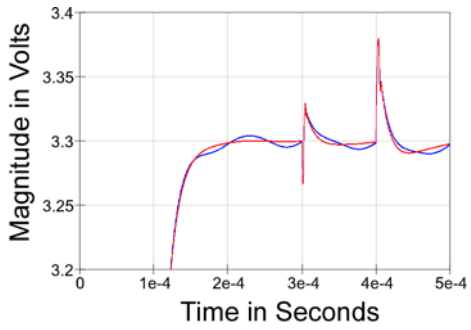

Figure 25.3 Buck Converter V_C Output Voltage Control Comparison

In figure 25.3, we illustrate the $\boldsymbol{V_C}$ output voltage for systems employing feedback alone in the blue trace versus both feedback and feedforward for the red trace. The differences are more perceptible on the relatively constant $\boldsymbol{V_C}$ output nominal values. The transient load step presents similar control problems to both because it is only the feedback of both that responds to load changes.

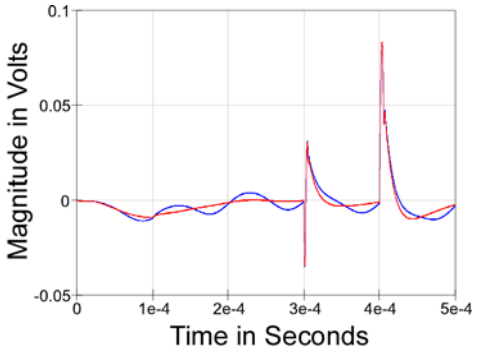

Figure 25.4 Buck Converter Error Voltage Control Comparison

In figure 25.4, we illustrate the error voltage for systems employing feedback alone in the blue trace versus both feedback and feedforward for the red trace. The differences are more obvious on the relatively constant V_{Error} signal values because the feedforward control greatly reduces the feedback control effort required. The transient load step presents similar control problems to both because it is only the feedback of both that responds to load changes.

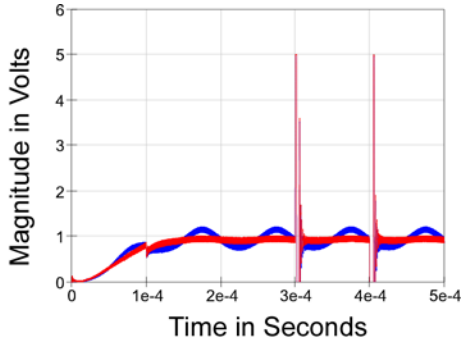

Figure 25.5 Buck Converter $V_{-Feedback}$ Voltage Control Comparison

In figure 25.5, we illustrate the feedback voltage to the PWM for systems employing feedback alone in the blue trace versus both feedback and feedforward for the red trace. The differences are very obvious on the relatively constant $V_{-Feedback}$ signal values because the feedforward control greatly reduces the feedback control effort required and the PZ compensator introduces a great deal of the loop-gain near the frequency of the disturbance. We see that without feedforward, there is a considerable feedback signal required at the PWM to reduce the effects of the disturbance. Again, the transient load step presents similar control problems to both because it is only the feedback of both that responds to load changes.

26.0 Summary and Conclusions

We have introduced a Switchmode Buck power conversion topology and shown considerations for selecting inductor and capacitor components essential for efficient energy transfer.

We analyzed the topologies for two states of switching and produced a state-space averaged model. We extracted a small-signal model and developed a linear model to examine potential stability issues. We included Zero-Order Hold (ZOH) effects of the discrete-time nature of the switch within the control loop, including extra phase contributions and the "notch" behavior near the Nyquist frequency. We designed Pole-Zero (PZ) compensators necessary to stabilize the open-loop characteristics of converters with disparate switching frequencies.

We introduced a Pulse-Width Modulator (PWM) and introduced it into the feedback loop. We added feedforward and feedback capabilities to the PWM and contrasted the efficacy of adding feedforward control to a feedback loop.

We have shown that a Buck converter can be designed using voltage feedback to meet the desired specifications.

A more complete design would also consider development of voltage reference components, power switching components, amplifier designs, supervisory startup circuits, component costs, and efficiency effects of component selection, but are beyond the scope of this course. The material covered should enable a working engineer to construct a stable Buck converter using voltage control.

